

Walter-Note Block Diagram

Project Code: 2014 July ' 10
PCB(Raw Card):

PCB Layer Stackup	
L1:TOP	
L2:GND1	
L3:Signal 1	
L4:GND 2	
L5:Signal 2	
L6:GND3	
L7:VCC1	
L8:Signal 3	
L9:VCC2	
L10:Signal 4	
L11:GND4	
L12:BOTTOM	
Battery Charger	
BQ24780SBUYR	88
INPUTS	OUTPUTS
DOCK_PWR20_F	M-BAT-PWR
System DC/DC	
TPS51285BRUKR	90
VINT20	VCC5M
	VCC3M
CPU DC/DC	
M: NCP81205MNTXG	91
S: NCP81382MNTXG	92, 93, 94
VINT20	VCCCPUCORE
	VCCGFXCORE_I
	VCCS4
VCCCPUIO	
NB681AGD-Z	95
VINT20	VCCCPUIO
VCC1R0_SUS	
SN1409027RVER	96
VCC5M	VCC1R0_SUS
VCC1R2A/VCC0R6B +SMDDR_VREF_DIMM	
TPS51716RUKR	99
VINT20	+SMDDR_VREF_DIMM
	VCC0R6B
	VCC1R2A
VCC1R8B	
BD9139MUV-E2	98
VCC5M	VCC1R8B
VCC2R5A	
BD91364BMU-E2	100
VCC5M	VCC2R5A
GFXCORE_D	
NCP81172MNTWG	110
VINT20	VCCGFXCORE_D
VCC1R35VIDEO	
TPS51219RTER	111
VCC5M	VCC1R35VIDEO
VCC1R05VIDEO	
NB681AGD-Z	112
VCC5M	VCC1R05VIDEO
	VCC1R05VIDEO_PL1

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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF	Hibernation or Shutdown	Soft Off
	S5	M3	ON	ON	ON	ON	OFF	OFF		
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G3	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off
	---	---	OFF	OFF	OFF	OFF	OFF	OFF		

Schematics Mark Definition

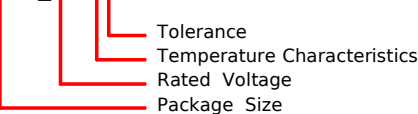
BOM Structure	BTO Item
@	Not assembled.
EMC@	Assembled. EMC related parts.
RF@	Assembled. RF related parts.
ME@	Assembled. ME related parts.
PRxxx, PCxxx, PLxxx	PWR related parts. If @, not assembled.
N16P@	Assembled. for N16P GPU SKU
N16S@	Assembled. for N16S GPU SKU
VP@	Assembled. for support vPro
NVP@	Assembled. Not support vPro

Any other mark like below is prohibited on Payton/Walter.
ESD@,EMI@,EMC_NS@,EMC_PX@,EMC_OPT@,CONN@,
CONN_NS@... RH,CH,LH(PCH related RLC)..

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX



Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
Bj	Ch	Cj	Ch	Sh	Sj	Uj	Uk	Sl	X5S	Noj

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device	Address
CH-A P DDR DIMM0	1001 0000b
CH-A S DDR DIMM1	1001 0001b
CH-B P DDR DIMM2	1001 0010b
CH-B S DDR DIMM3	1001 0011b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

CPU



PCB



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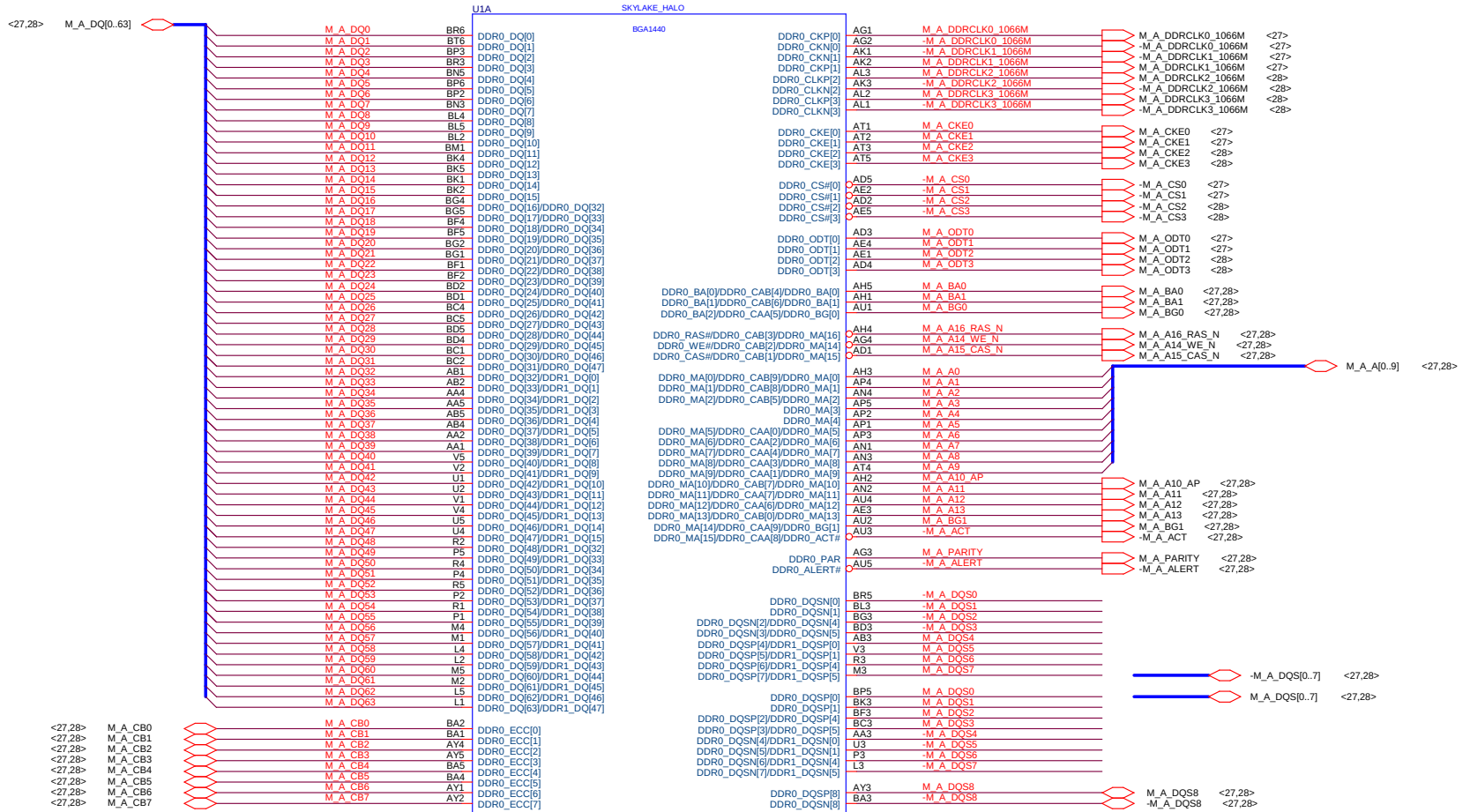
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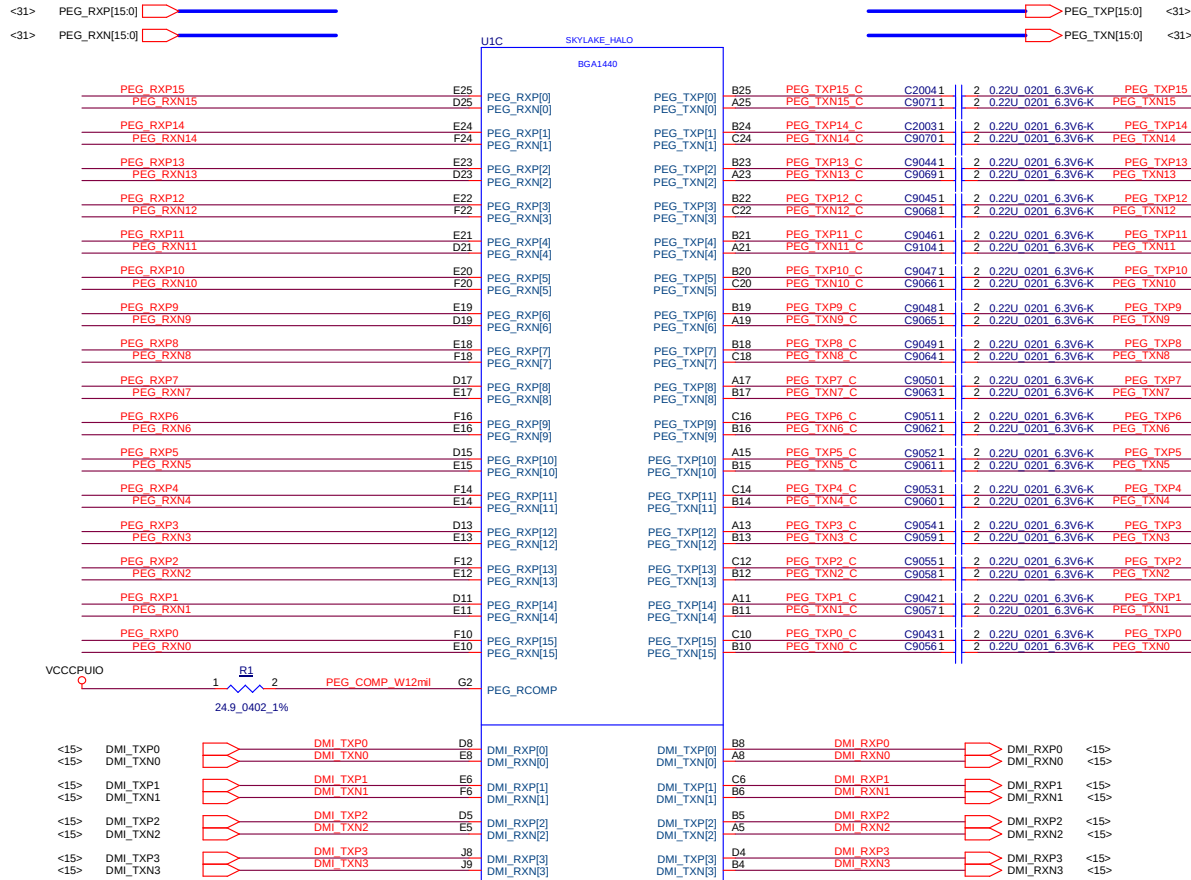
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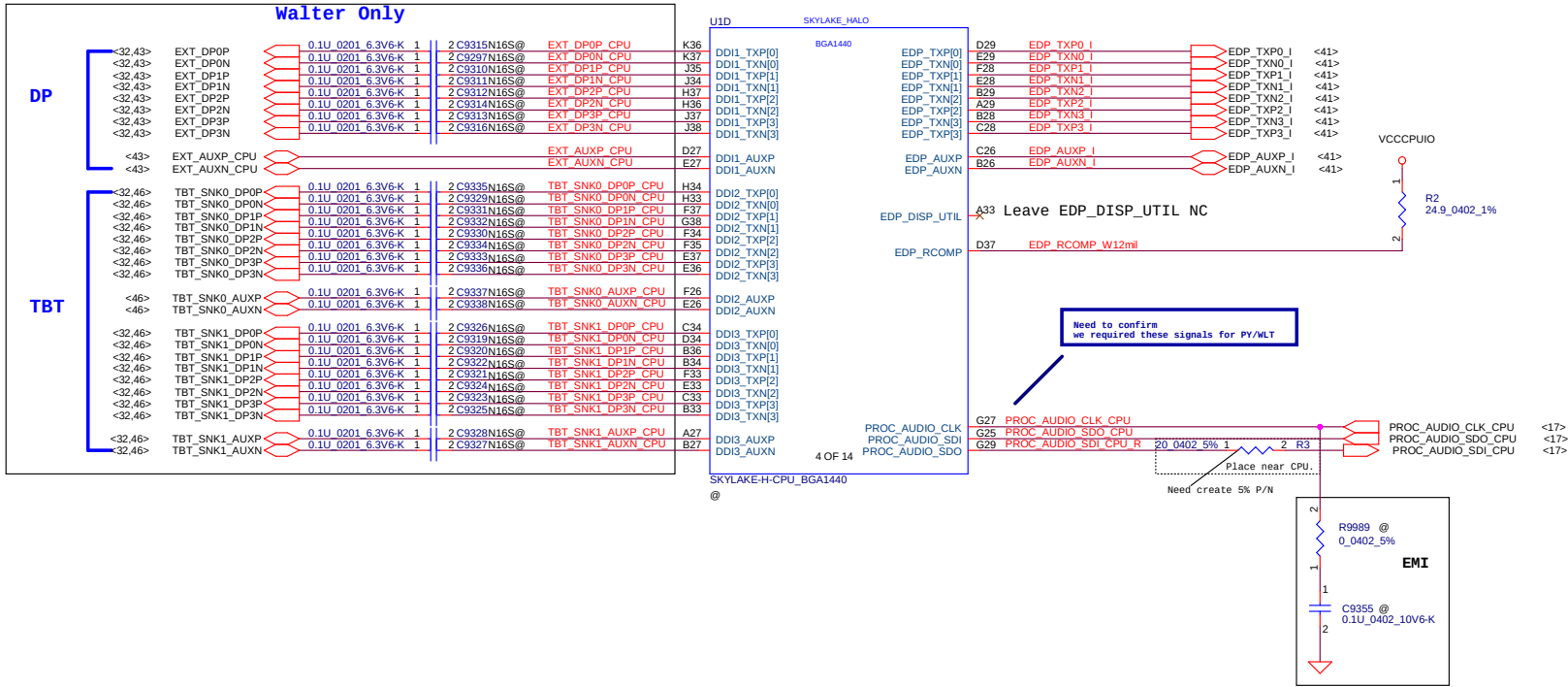
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DDR4 INTERLEAVE IMPLEMENTATION

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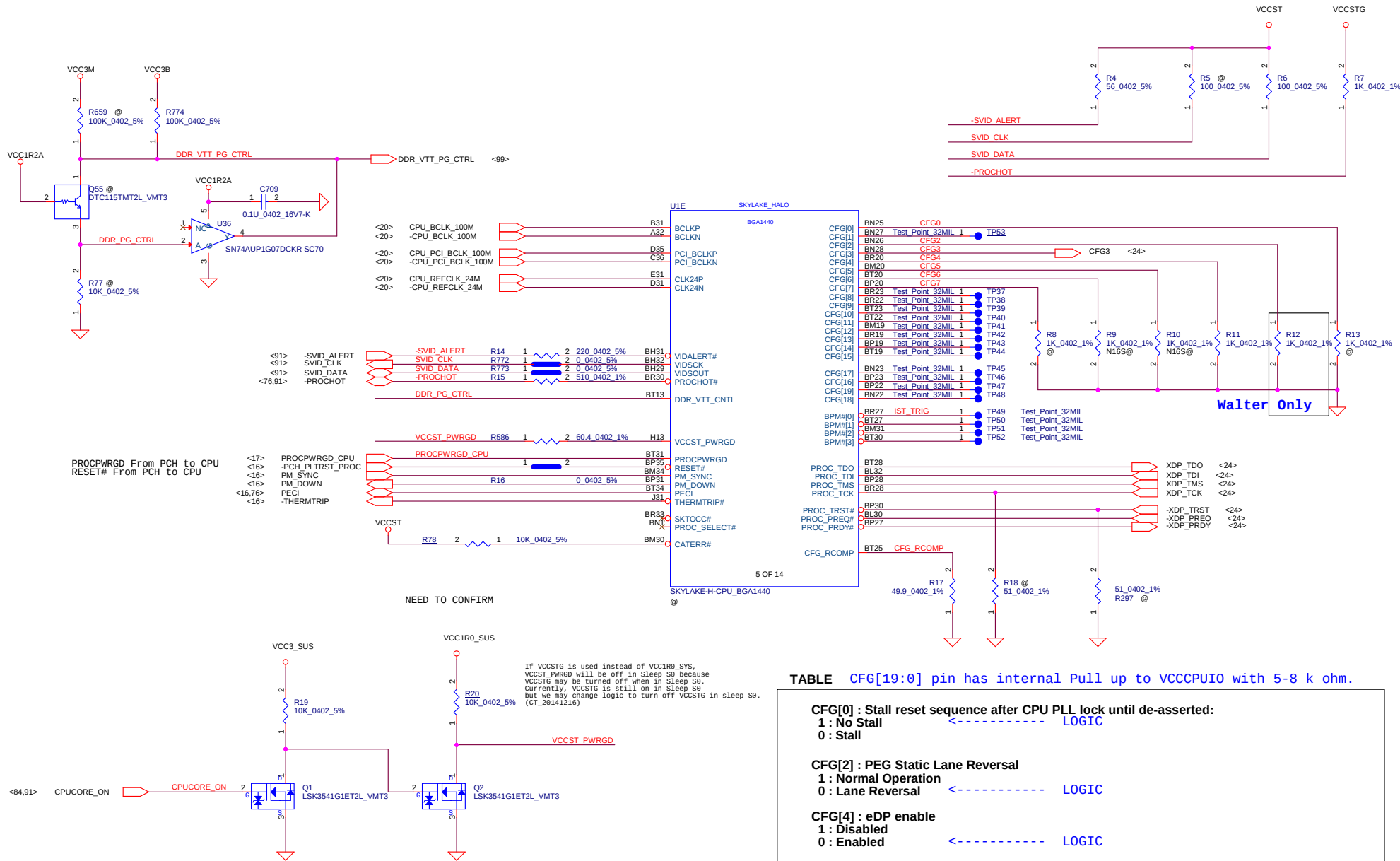
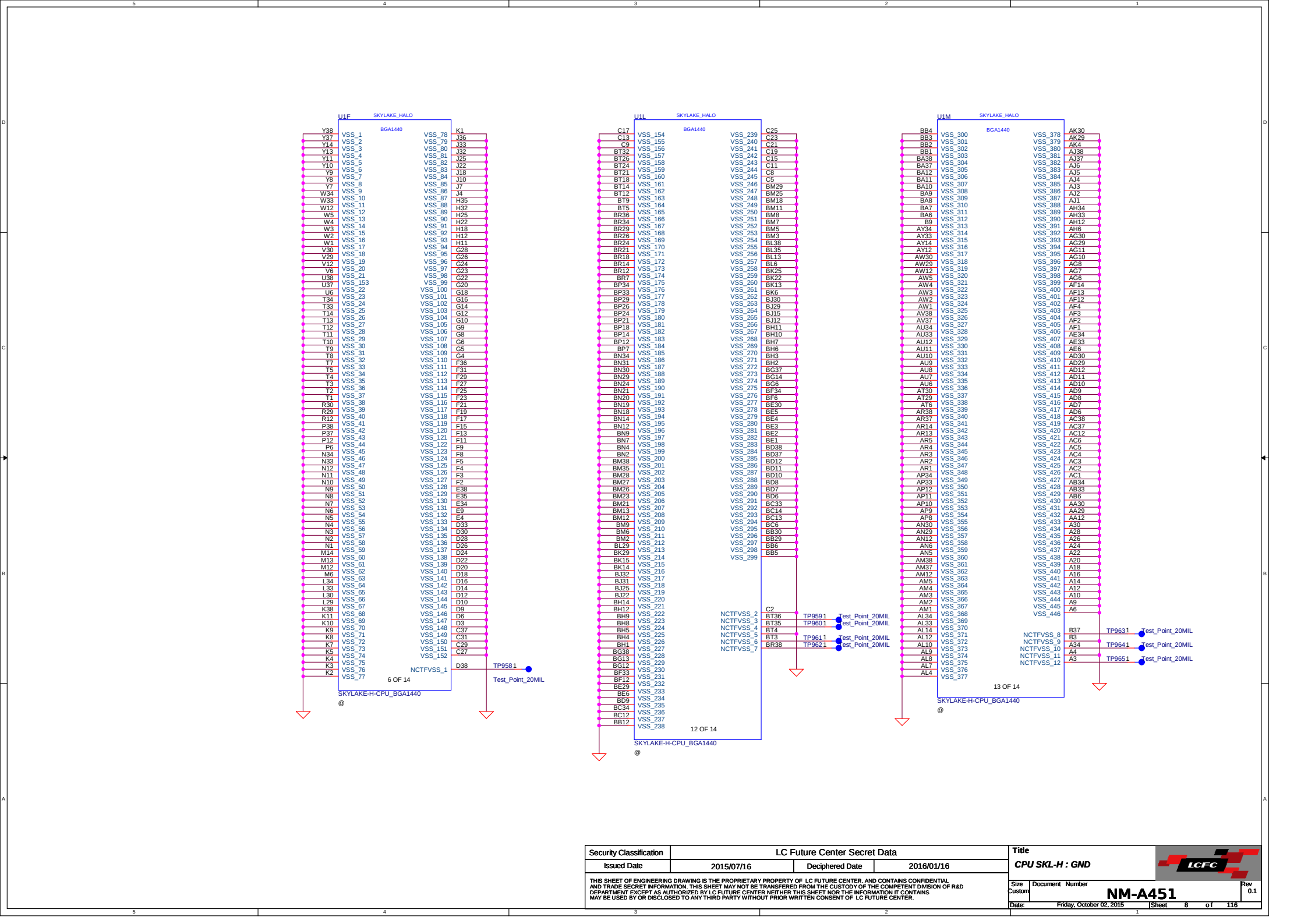
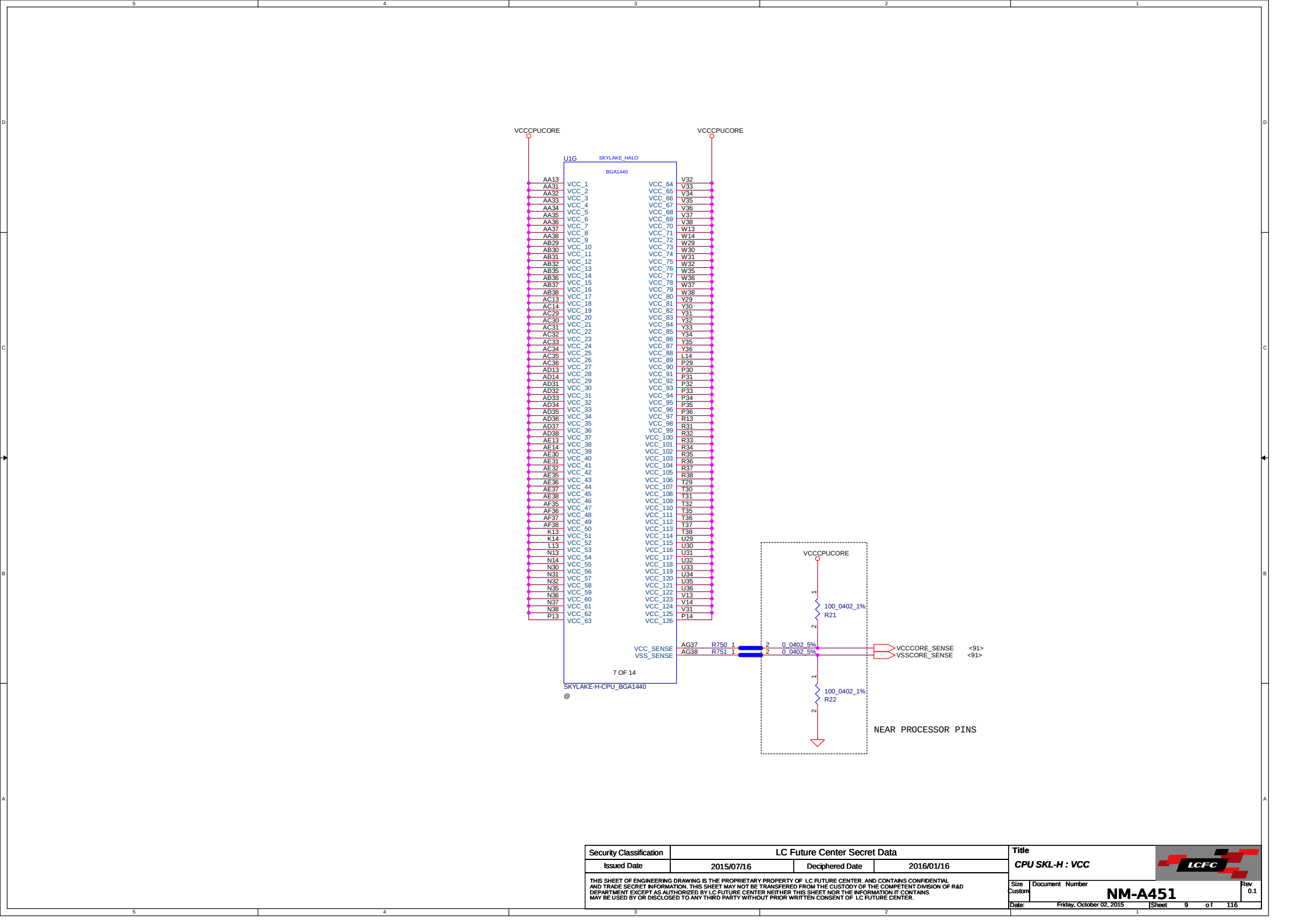
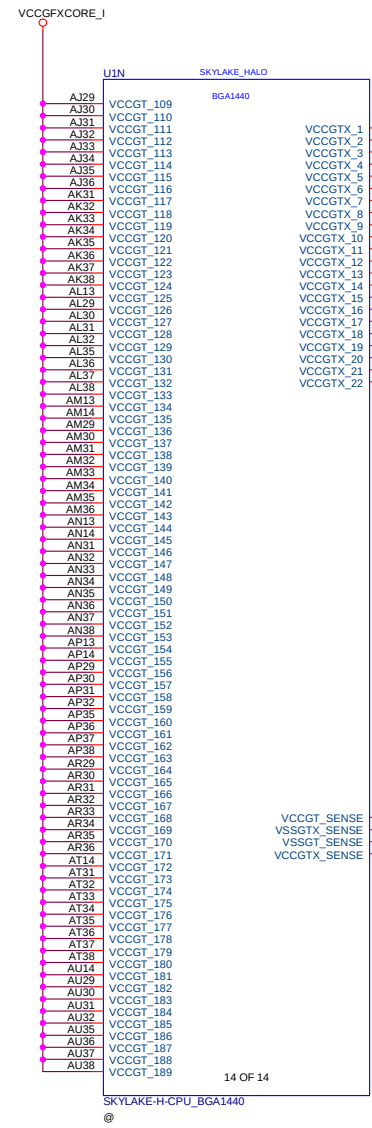
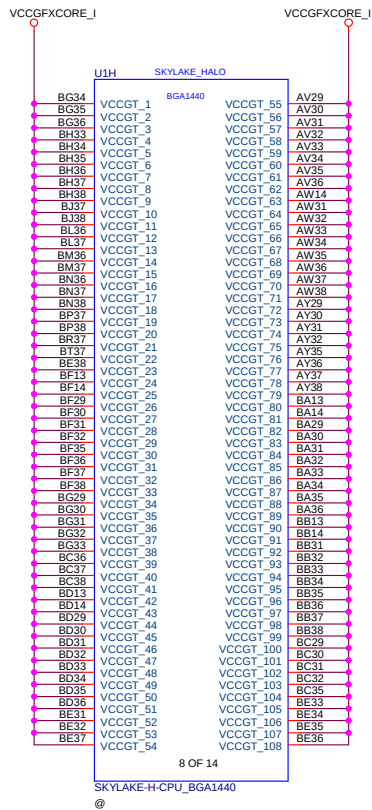


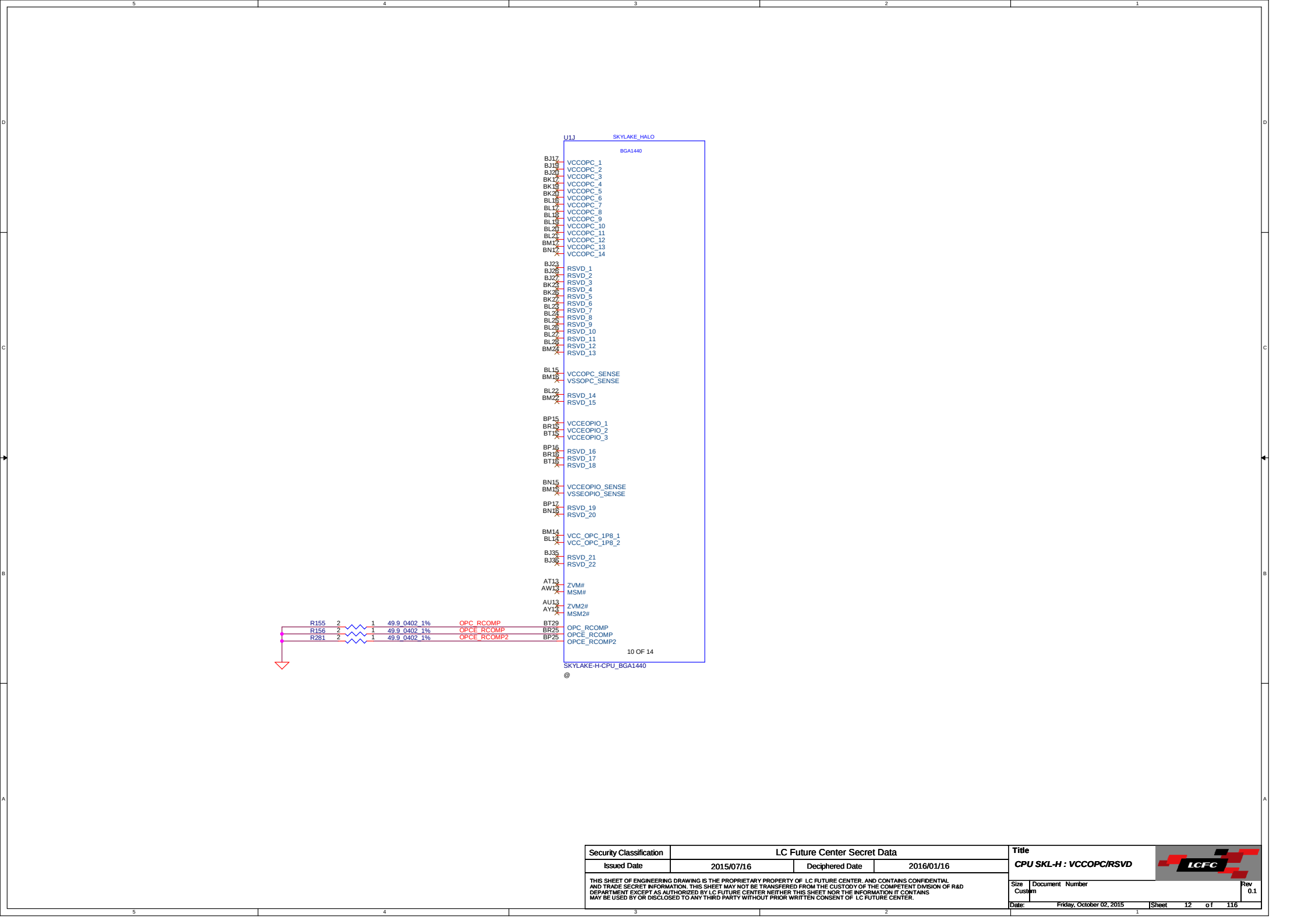
TABLE CFG[19:0] pin has internal Pull up to VCCCPUI0 with 5-8 k ohm.

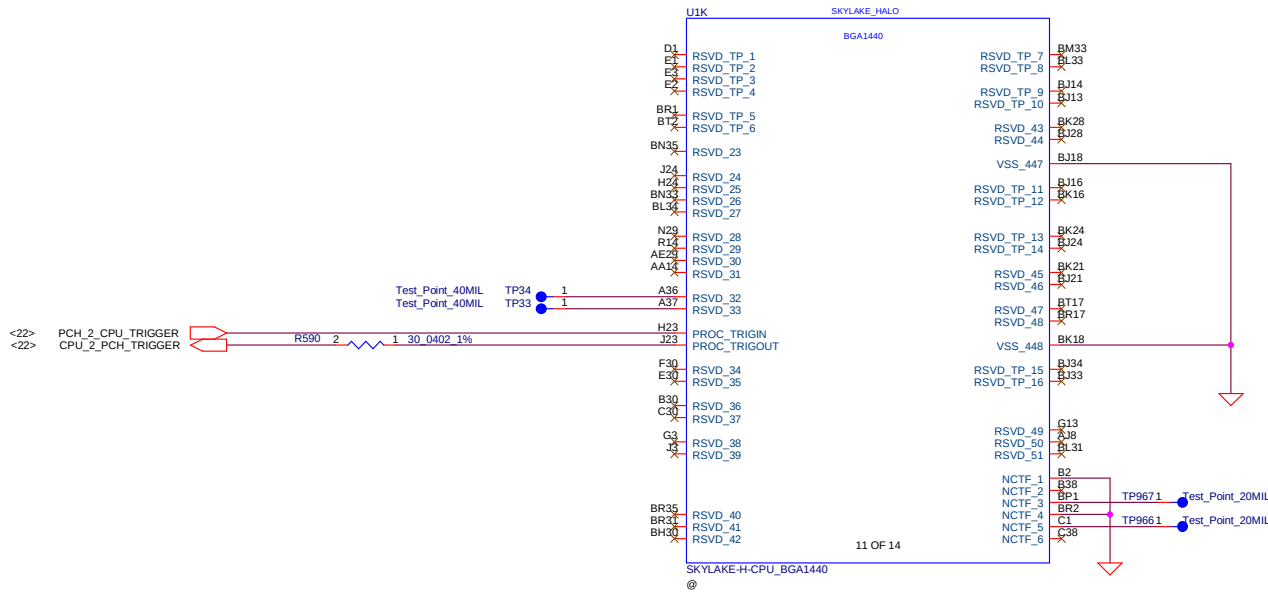
CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:	
1 : No Stall	LOGIC
0 : Stall	
CFG[2] : PEG Static Lane Reversal	
1 : Normal Operation	
0 : Lane Reversal	LOGIC
CFG[4] : eDP enable	
1 : Disabled	LOGIC
0 : Enabled	
CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0	
11 : 1x16	LOGIC
CFG[7] : PEG Training	
1 : PEG Train immediately following RESET# deassertion	LOGIC
0 : PEG Wait for BIOS for training	
CFG[19:8] : Reserved	
For x16 Reversal Lanes - CFG[6/5/2] setting is 110	
For x4 Reversal Lanes - CFG[6/5/2] setting is 000	




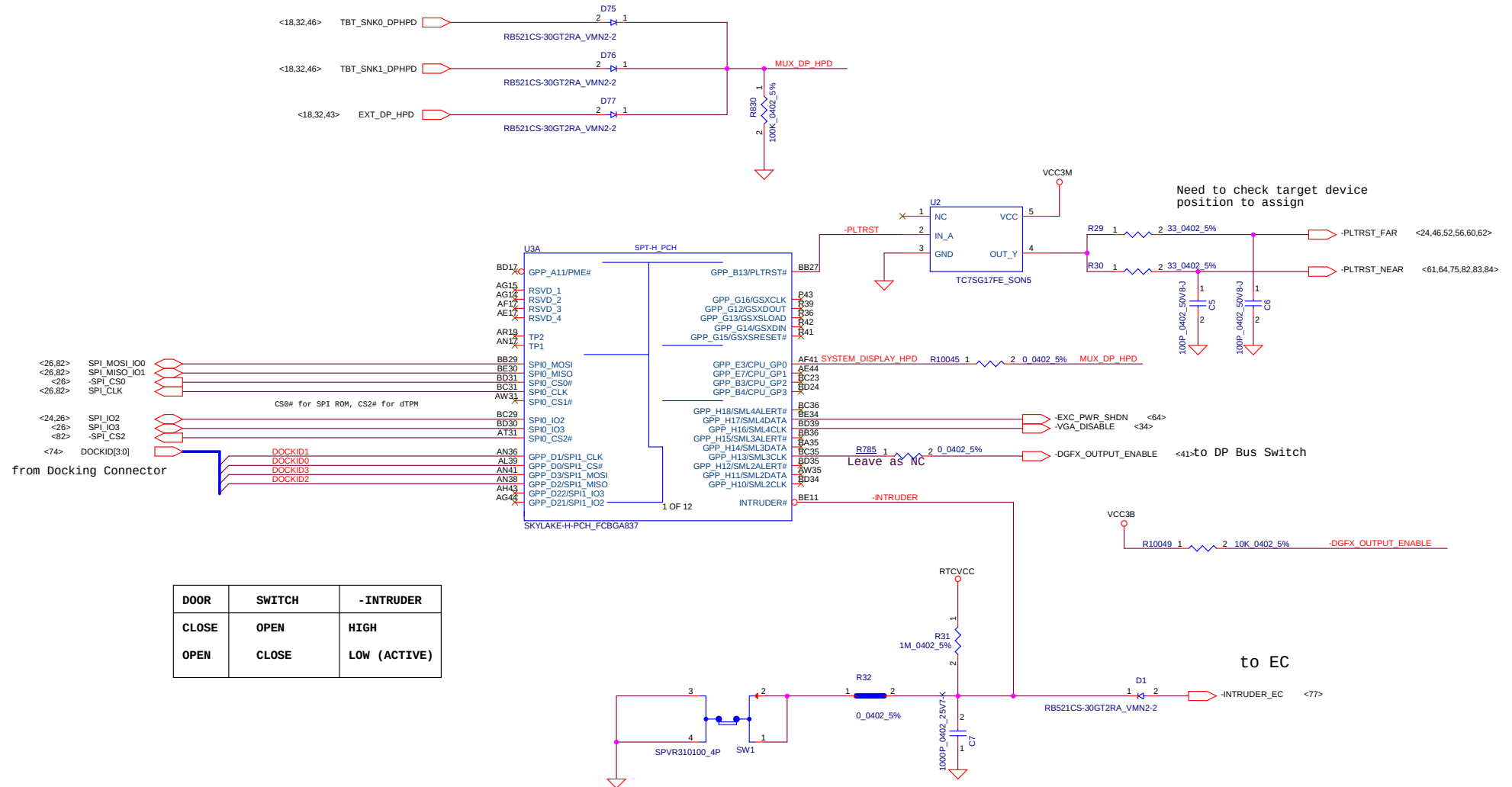








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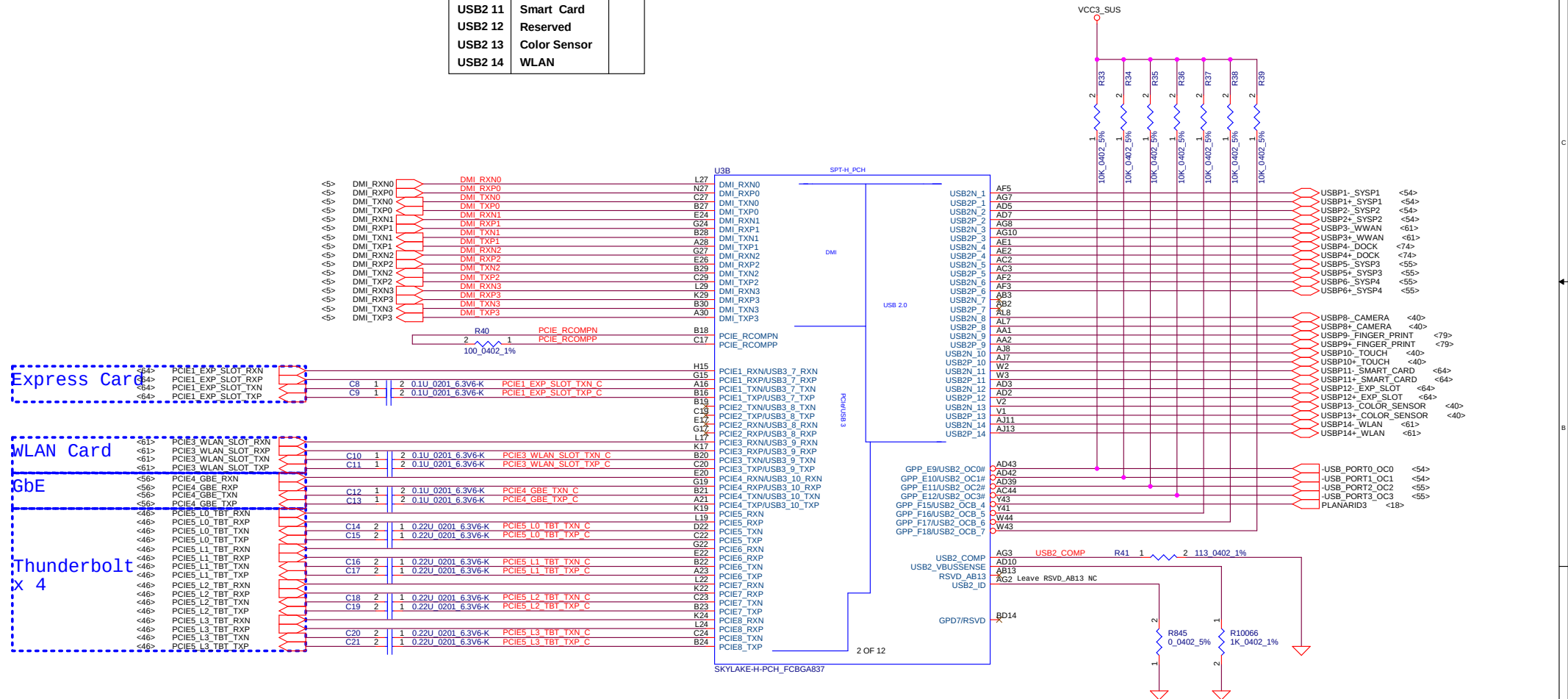



Flexible I/O Configuration (v0.51)			
I/O	High Speed Signals	Configuration	Net Name
Port 1 - 6		Please see Page 19	
Port 7	USB3 7 / PCIE 1	USB3 7 or PCIE 1	PCIE1_EXP_SLOT
Port 8	USB3 8 / PCIE 2	USB3 8	
Port 9	USB3 9 / PCIE 3	PCIE 3	PCIE3_WLAN_SLOT
Port 10	USB3 10 / PCIE 4 (GBE)	GBE	PCIE4_GBE
Port 11	PCIE 5 (GBE)	PCIE 5	PCIE5_L0_TBT
Port 12	PCIE 6	PCIE 6	PCIE5_L1_TBT
Port 13	PCIE 7	PCIE 7	PCIE5_L2_TBT
Port 14	PCIE 8	PCIE 8	PCIE5_L3_TBT

USB2.0 Configuration (v0.51)		
USB2 #	Assignment	OCx #
USB2 1	System Port 1	0
USB2 2	System Port 2	1
USB2 3	WWAN	
USB2 4	DOCK	
USB2 5	System Port 3	2
USB2 6	System Port 4	3
USB2 7	Reserved	
USB2 8	Camera	
USB2 9	Finger print	
USB2 10	Touch panel	
USB2 11	Smart Card	
USB2 12	Reserved	
USB2 13	Color Sensor	
USB2 14	WLAN	

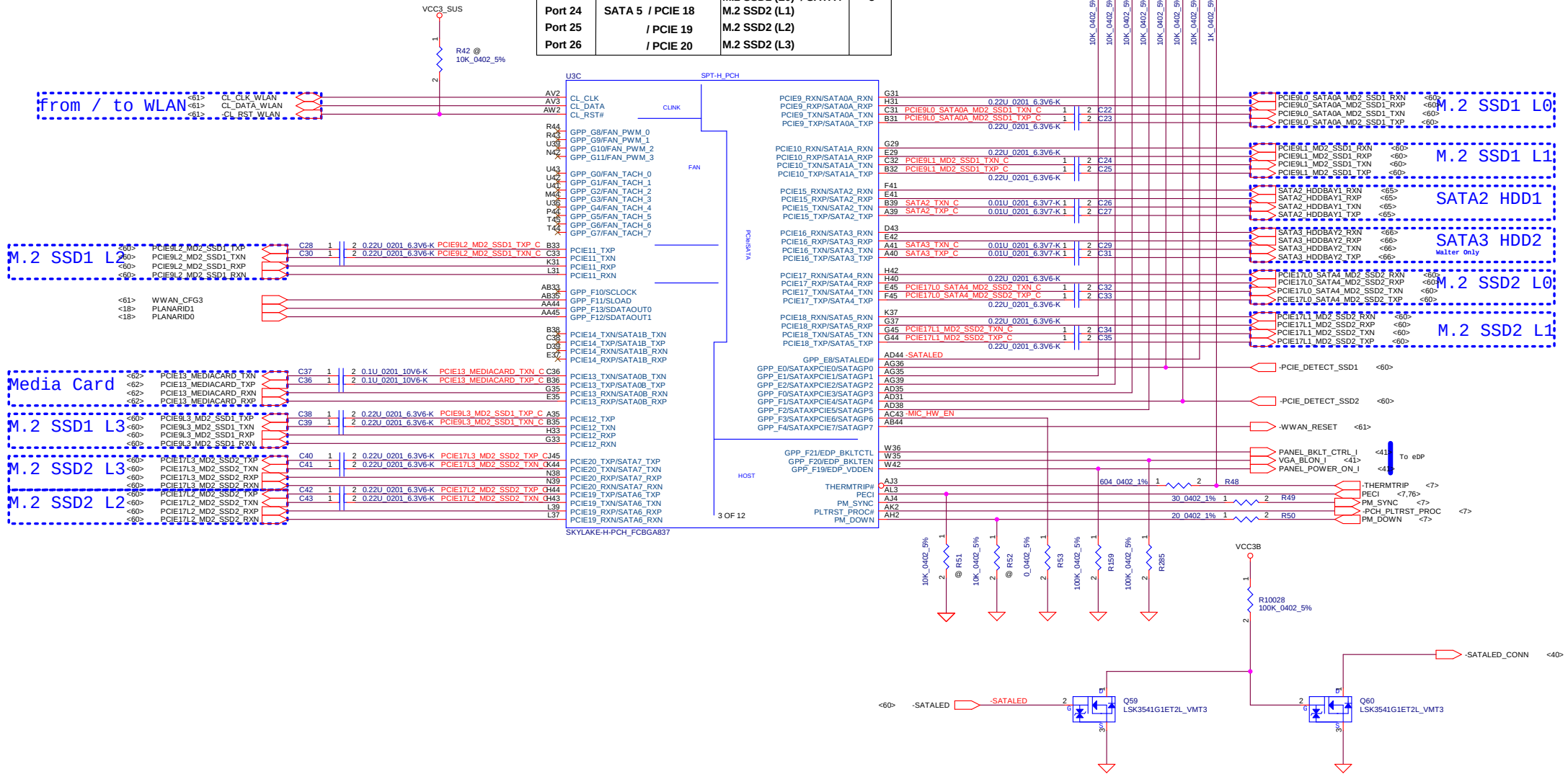
PCIE Configuration (v0.51)		
PCIE #	High Speed Signals	GEN
PCIE 1		
PCIE 2		
PCIE 3	WLAN Card	2
PCIE 4	GBE	
PCIE 5	Thunderbolt 1	3
PCIE 6	Thunderbolt 2	
PCIE 7	Thunderbolt 3	
PCIE 8	Thunderbolt 4	
PCIE 9 - 20	Please see Page 16	

USB3.0 Configuration (v0.51)	
USB 3#	High Speed Signals
USB3 1 - 6	Please see Page 19
USB3 7	
USB3 8	
USB3 9	
USB3 10	



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PCIE / SATA Configuration (v0.51)				
I/O	High Speed Signals	Configuration	GEN	
Port 15	SATA 0A / PCIE 9	M.2 SSD1 (L0) / SATA0A	3/3	
Port 16	SATA 1A / PCIE 10	M.2 SSD1 (L1)		
Port 17	/ PCIE 11	M.2 SSD1 (L2)		
Port 18	/ PCIE 12	M.2 SSD1 (L3)		
Port 19	SATA 0B / PCIE 13	Media Card	2	
Port 20	SATA 1B / PCIE 14	Reserved	---	
Port 21	SATA 2 / PCIE 15	SATA2 for HDD1	3	
Port 22	SATA 3 / PCIE 16	SATA3 for HDD1	3	
Port 23	SATA 4 / PCIE 17	M.2 SSD2 (L0) / SATA4	3	
Port 24	SATA 5 / PCIE 18	M.2 SSD2 (L1)		
Port 25	/ PCIE 19	M.2 SSD2 (L2)		
Port 26	/ PCIE 20	M.2 SSD2 (L3)		



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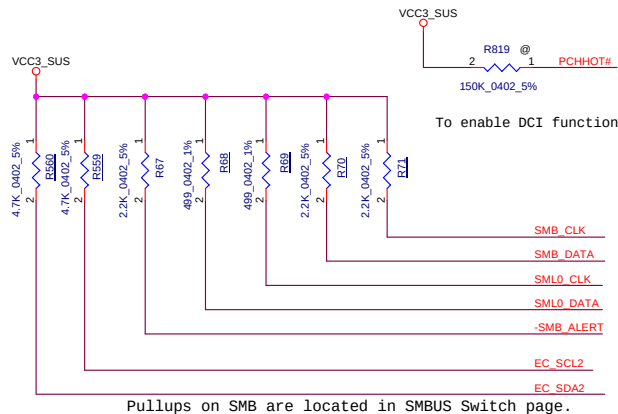
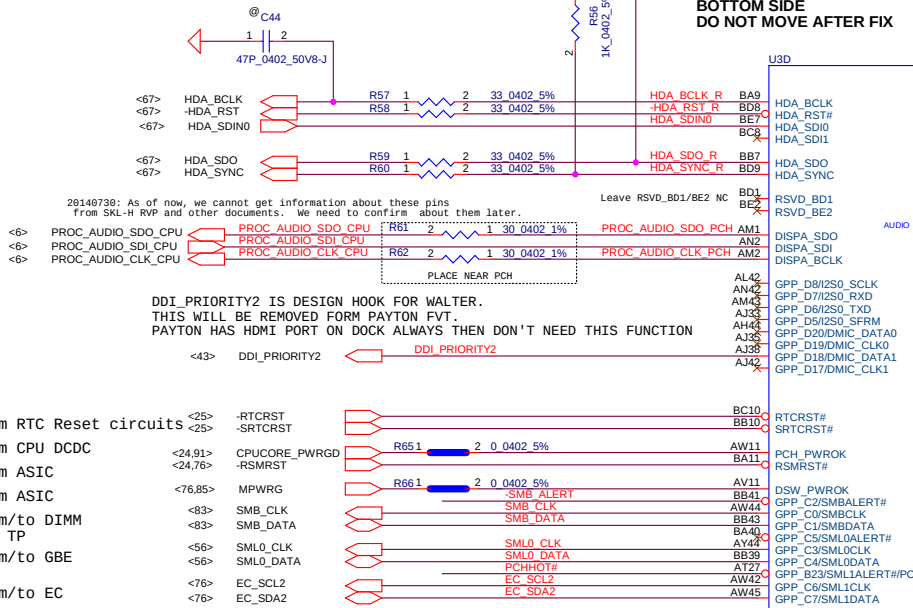
HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

PLACE ON BOTTOM SIDE

1 R54 2 1 R55 @ 2
1K_0402_5% 0_0402_5%

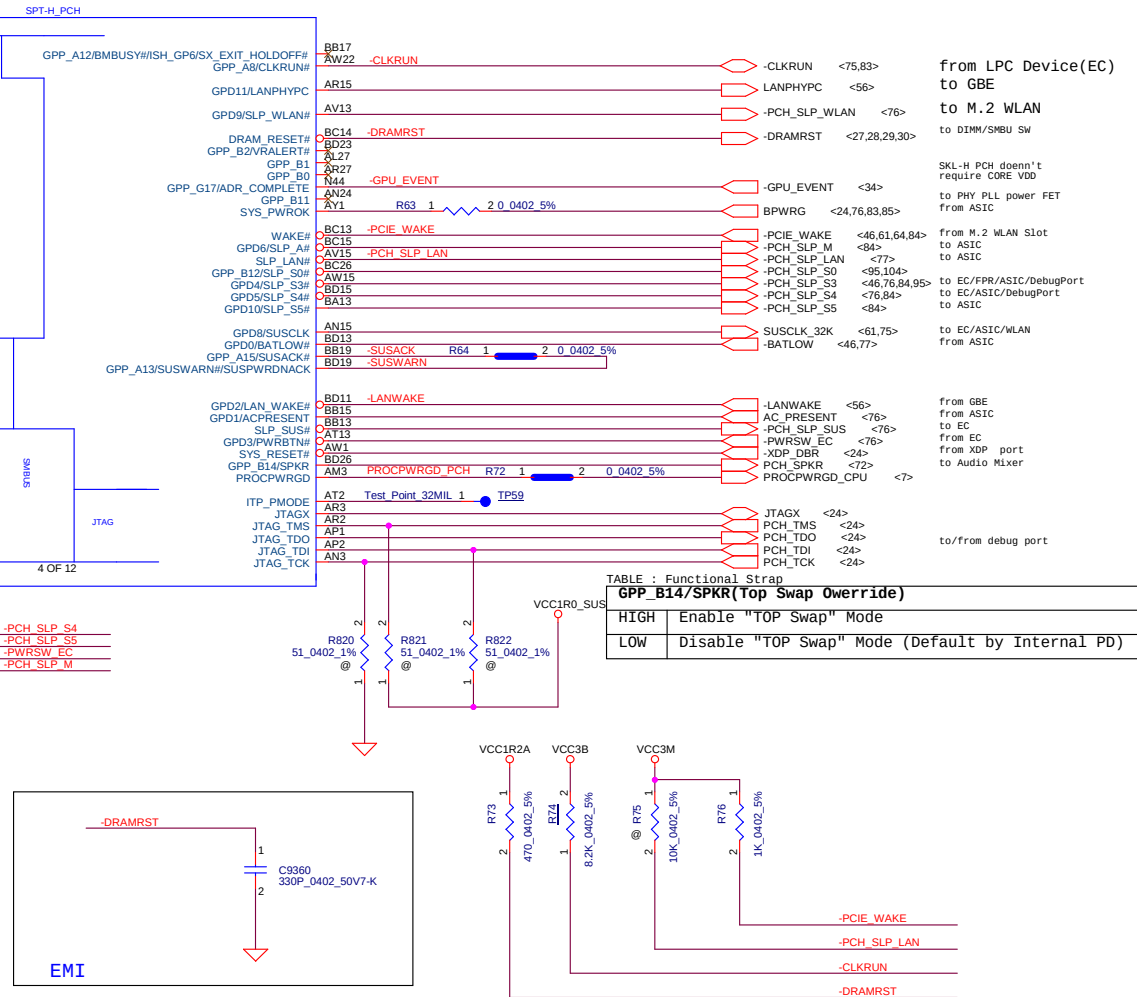
1 TP5 TP6 1
Test_Point_20MIL Test_Point_20MIL

**TEST PAD
BOTTOM SIDE
DO NOT MOVE AFTER FIX**




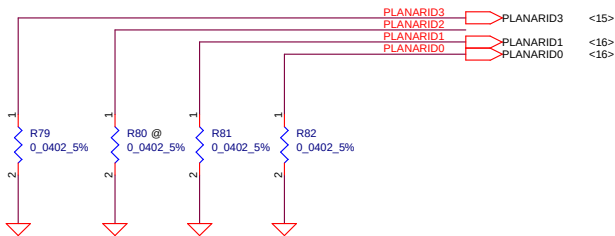
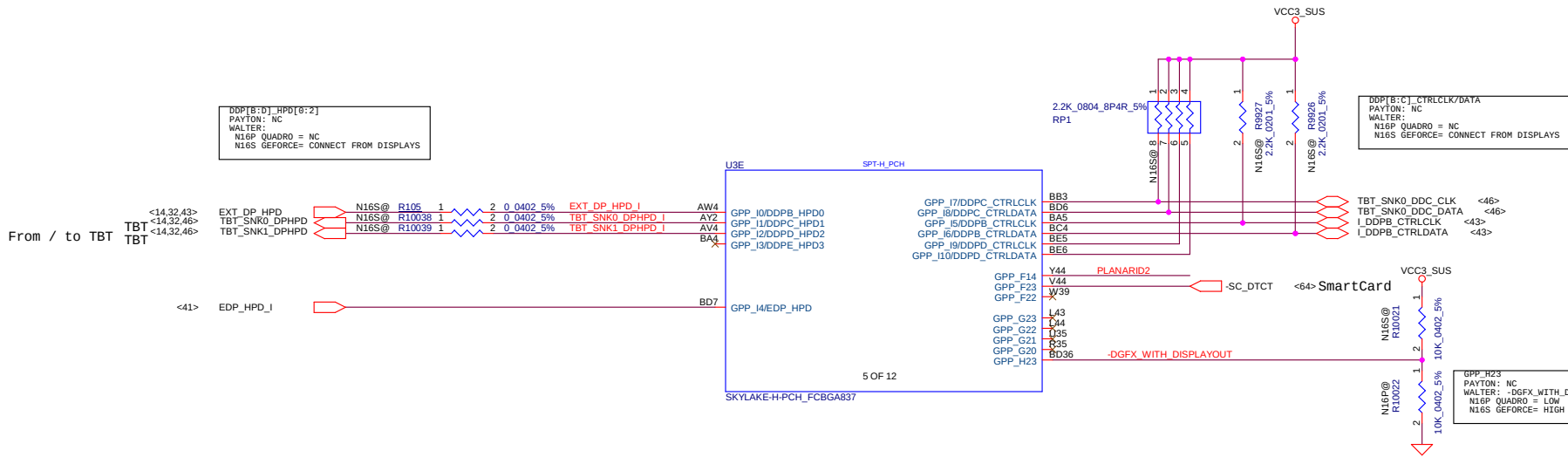
GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS(Default)



SUS	GPP_B14/SPKR(Top Swap Override)	
	HIGH	Enable "TOP Swap" Mode
	LOW	Disable "TOP Swap" Mode (Default by Internal PD)

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TABLE

	PLANAR ID			
	3	2	1	0
	R79	R80	R81	R82
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3..0]	CPU	PCH
PDV	-----	-----	-----
SDV	0001b	ES(Q0)	ES2(C0)
FVT	0010b	ES(Q0)	ES2(C0)
SIT	0011b	QS(R0)	QS(D1)
SIT-4G	0011b	QS(R0)	QS(D1)
SIT-2	0011b	QS(R0)	QS(D1)
SVT	0100b	Prod	Prod

Configuration	-DGFX_WITH_DISPLAYOUT	-DGFX_OUTPUT_DISPLAYOUT	dGFX_output	iGFX_output
N16S	H	H		eDP,mDP,TBT
N16S / (Invalid)	H	L		mDP,TBT
N16P	L	H	mDP,TBT	eDP
N16P	L	L	eDP,mDP,TBT	


(P.14)

<7> CPU_REFCLK_24M
<7> -CPU_REFCLK_24M
<7> CPU_BCLK_100M
<7> -CPU_BCLK_100M

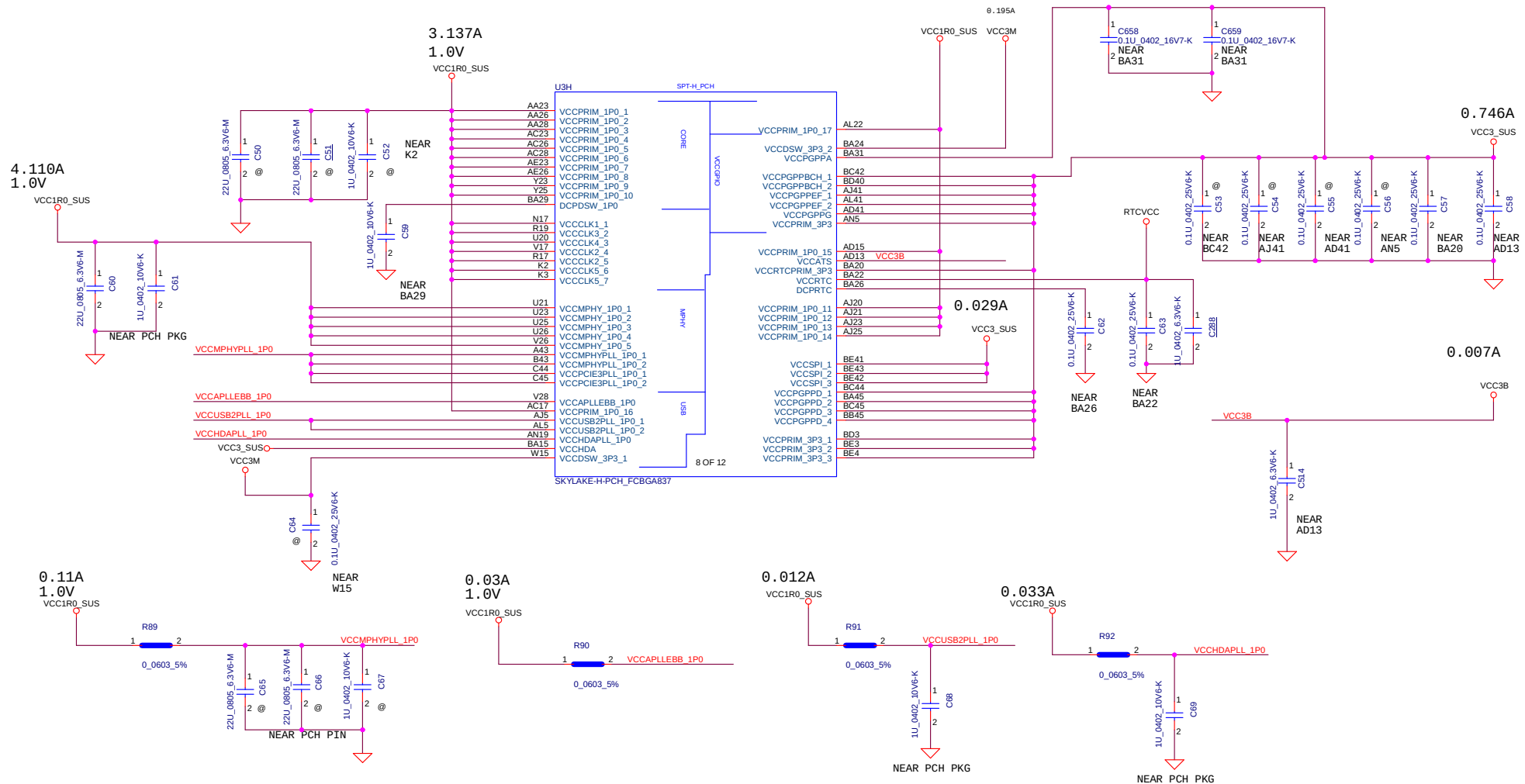
<62> -CLKREQ_PCIE0_UHS2
<61> -CLKREQ_PCIE2_WLAN
<56> -CLKREQ_PCIE3_GBE
<60> -CLKREQ_PCIE4_MD2_SSD1
<31> -CLKREQ_PCIE5_PEG
<64> -CLKREQ_PCIE6_EXPCARD
<60> -CLKREQ_PCIE7_MD2_SSD2
<46> -CLKREQ_PCIE8_TBT

External Pull on CLKREQ# should be placed in device page,
as power rails may be different from PCH-H..

PCIE Clock Assignment
Clock 0 : UHS II
Clock 1 : NA
Clock 2 : Wireless LAN M.2 Slot
Clock 3 : Giga Bit Ethernet
Clock 4 : PCIe SSD on M.2 Slot
Clock 5 : Discrete GFX(MXM or Onboard)
Clock 6 : Express Slot
Clock 7 : PCIe SSD on M.2 slot
Clock 8 : Thunderbolt
Clock 9 - 15 : NA

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To use eSPI, VCCPGPPA should have 1.8V



Note 1: Ampere in this page means Iccmax current described in SKL PCH H EDS r0.91 page 57.

Note 2: Decoupling capacitors refers SKL H PDG r0.7 page 507.
SKL H RVP11 schematics r0.5 also referred.

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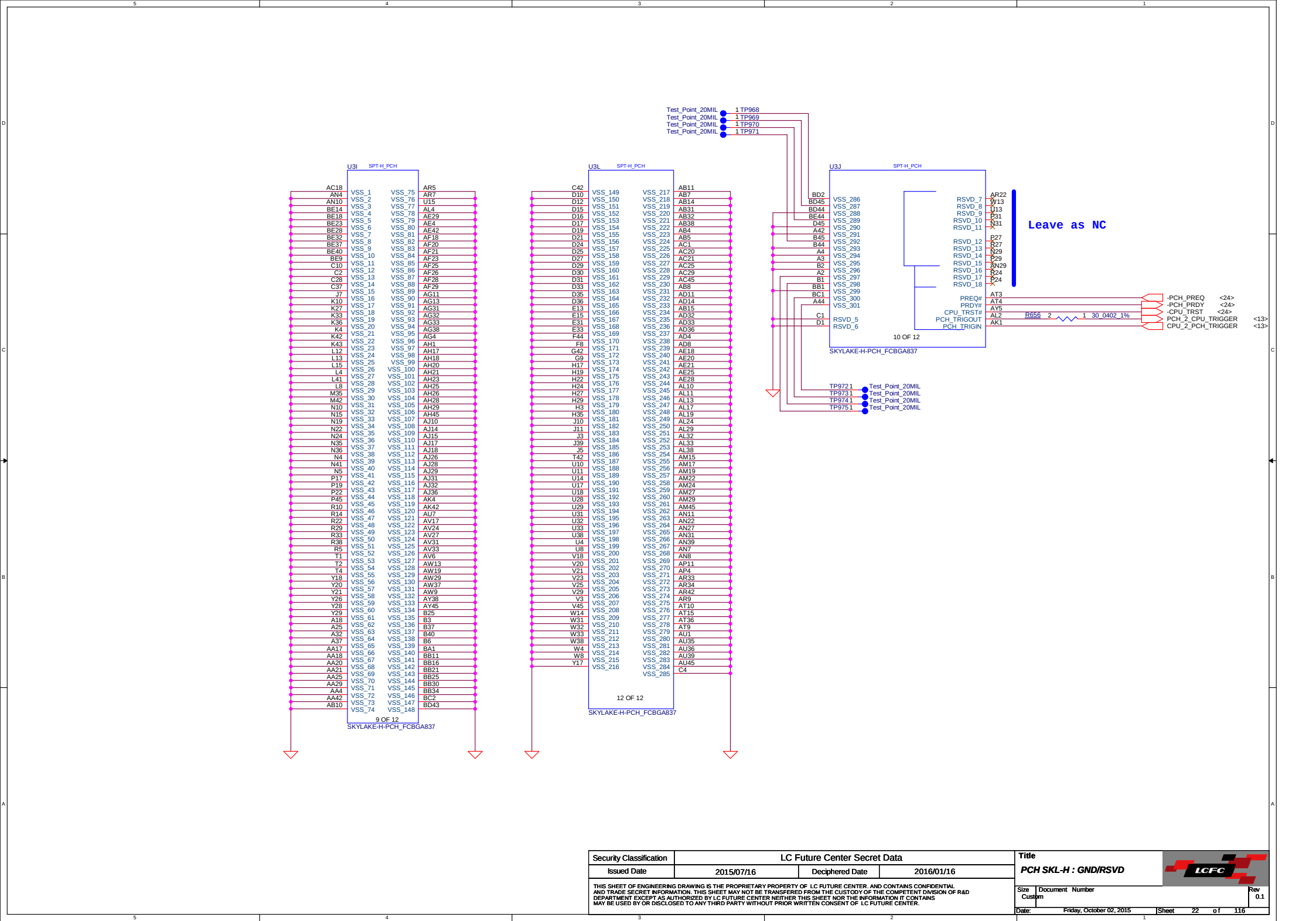


TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	ASM	ASM	ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

TABLE : PCH ITP DEBUG REPORT

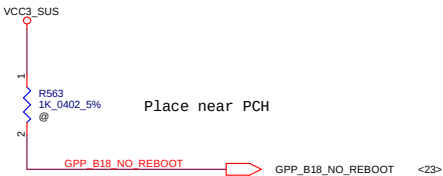
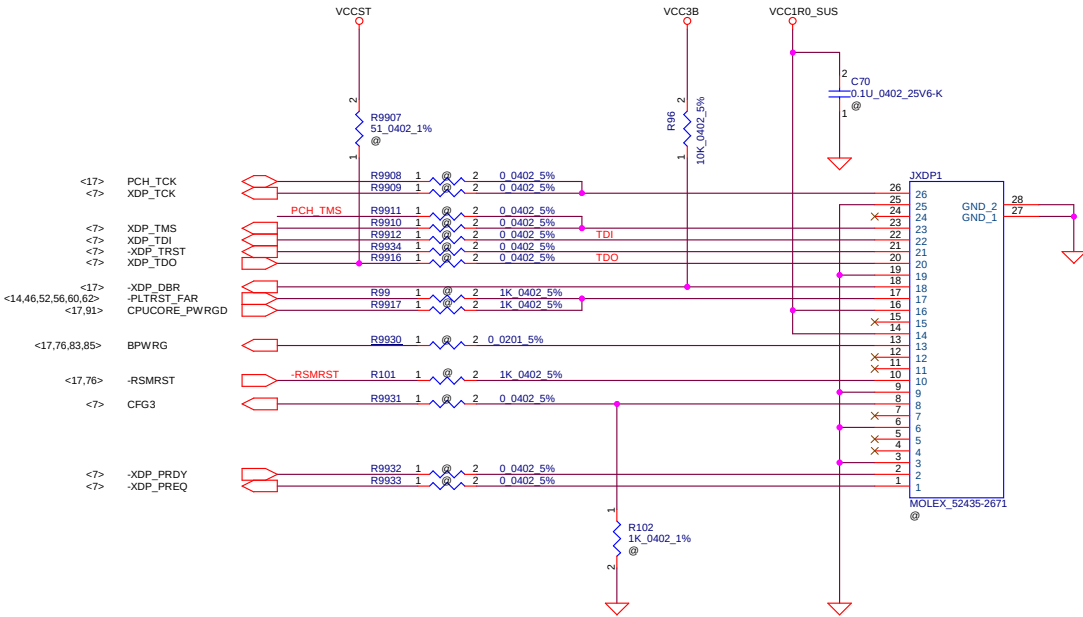
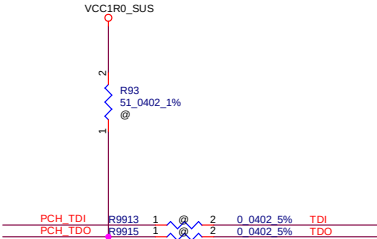
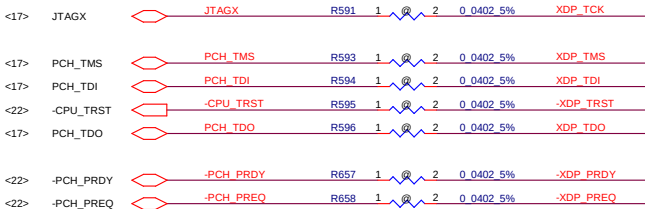
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

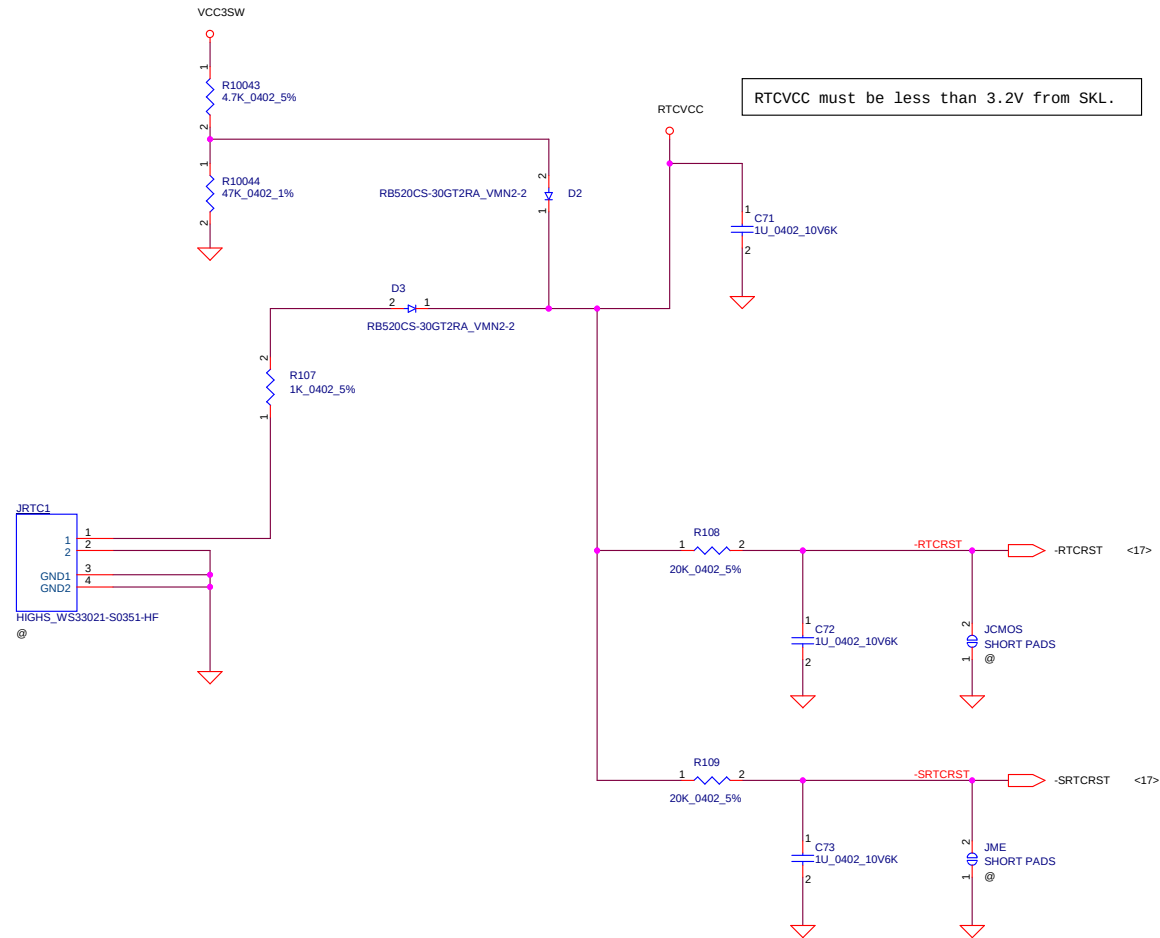
R820	NO ASM	ASM	NO ASM
R821	NO ASM	ASM	NO ASM
R822	NO ASM	ASM	NO ASM

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

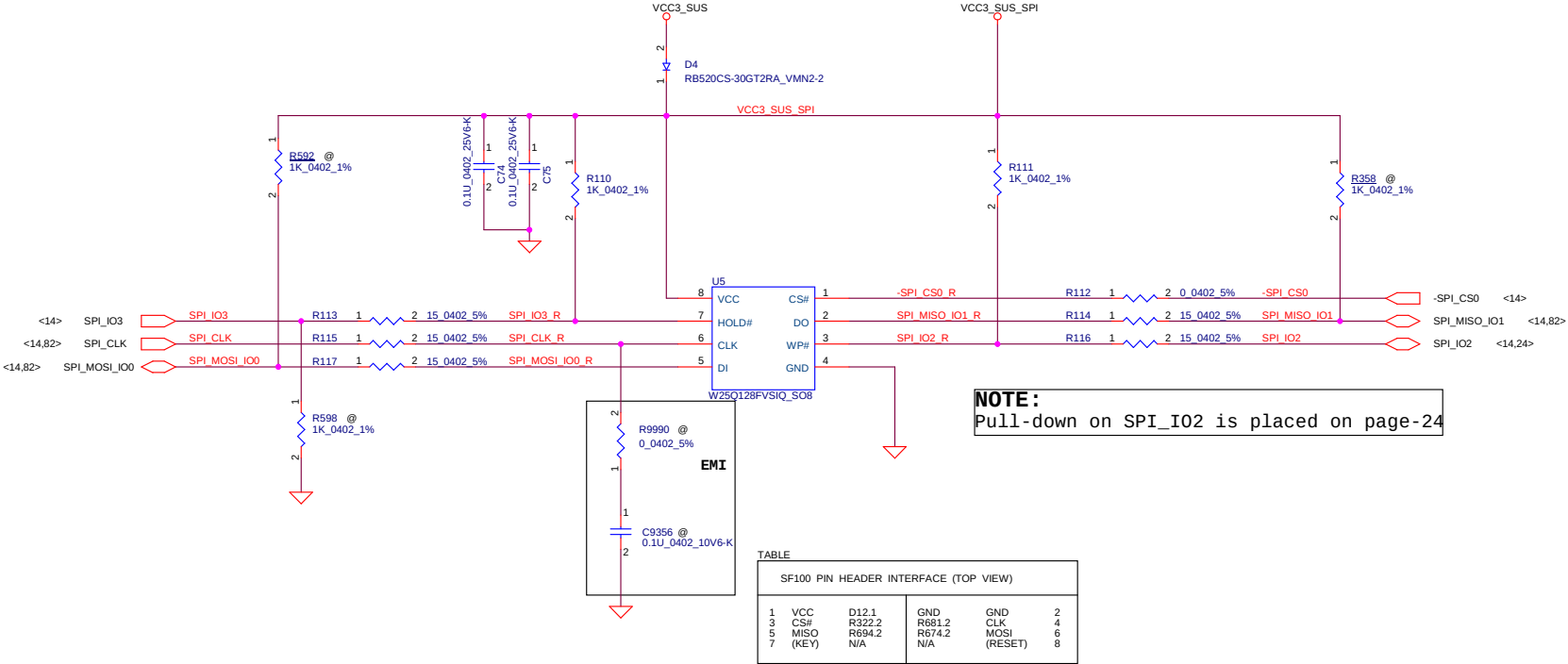
SHEET 17





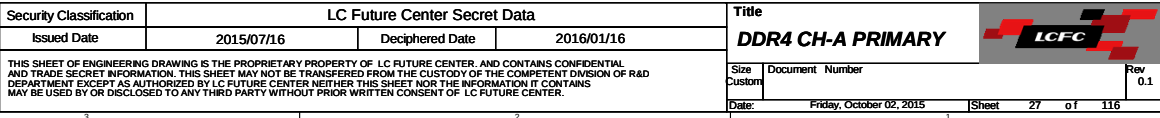
	R110	R598	U5	R592	R358
PRE ES1 ES1/ES2	NO ASM	ASM	QE="1"	ASM	ASM
AFTER QS	ASM	NO ASM	QE= Don't Care	NO ASM	NO ASM

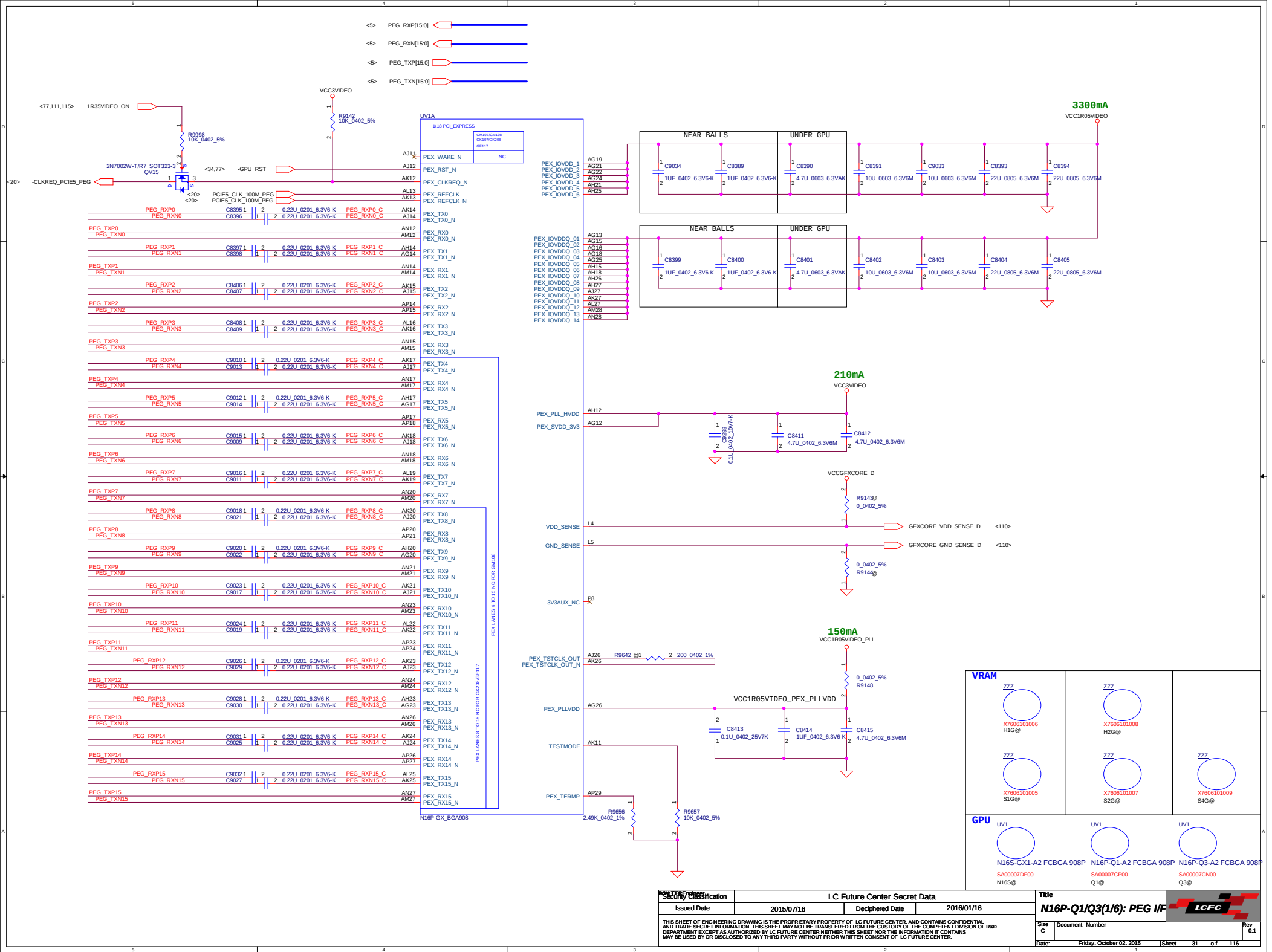
← LOGIC

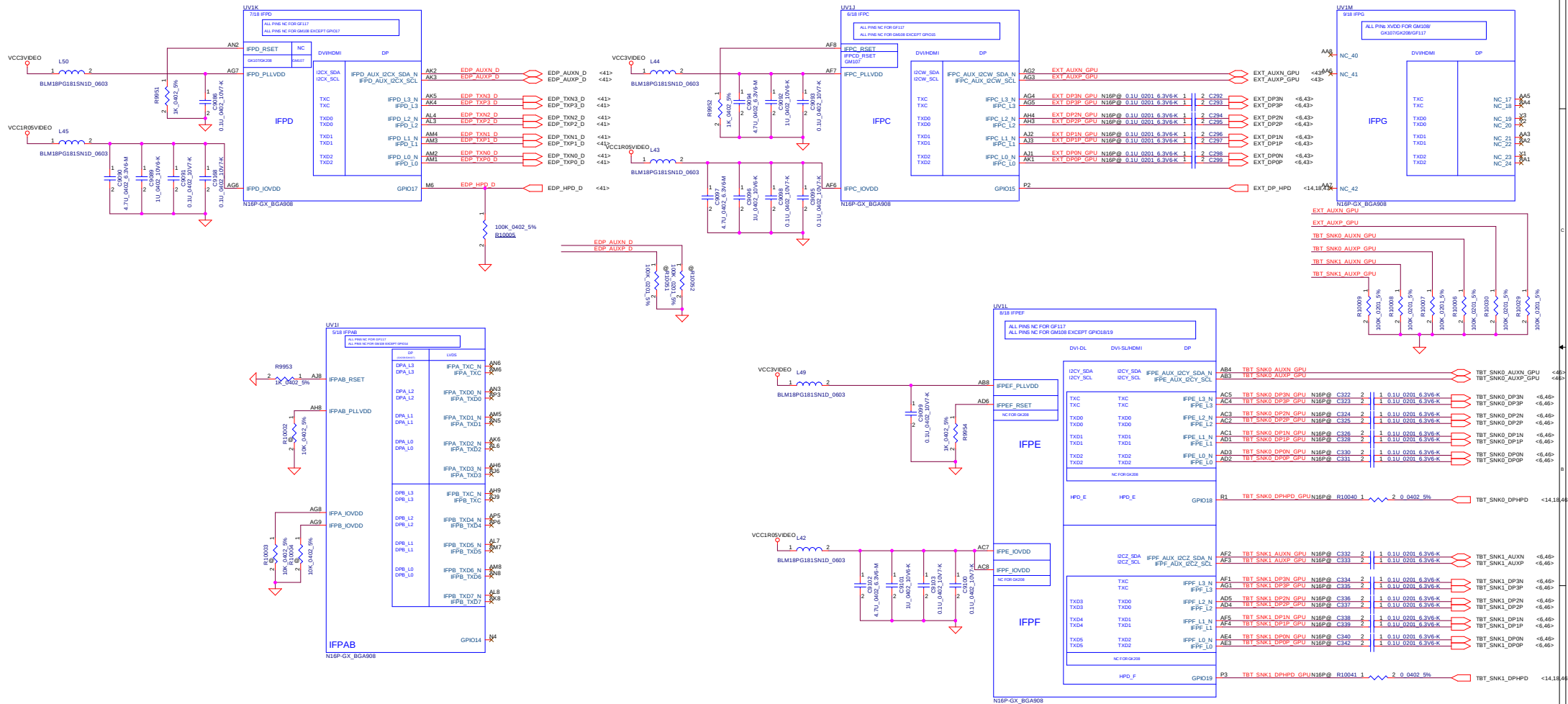


U5 SPI ROM
vPRO model(16MB)
WINBOND W25Q128FVSIQ MACRONIX MX25L12873FM2I-10G MICRON N25Q128A13ESEDFF

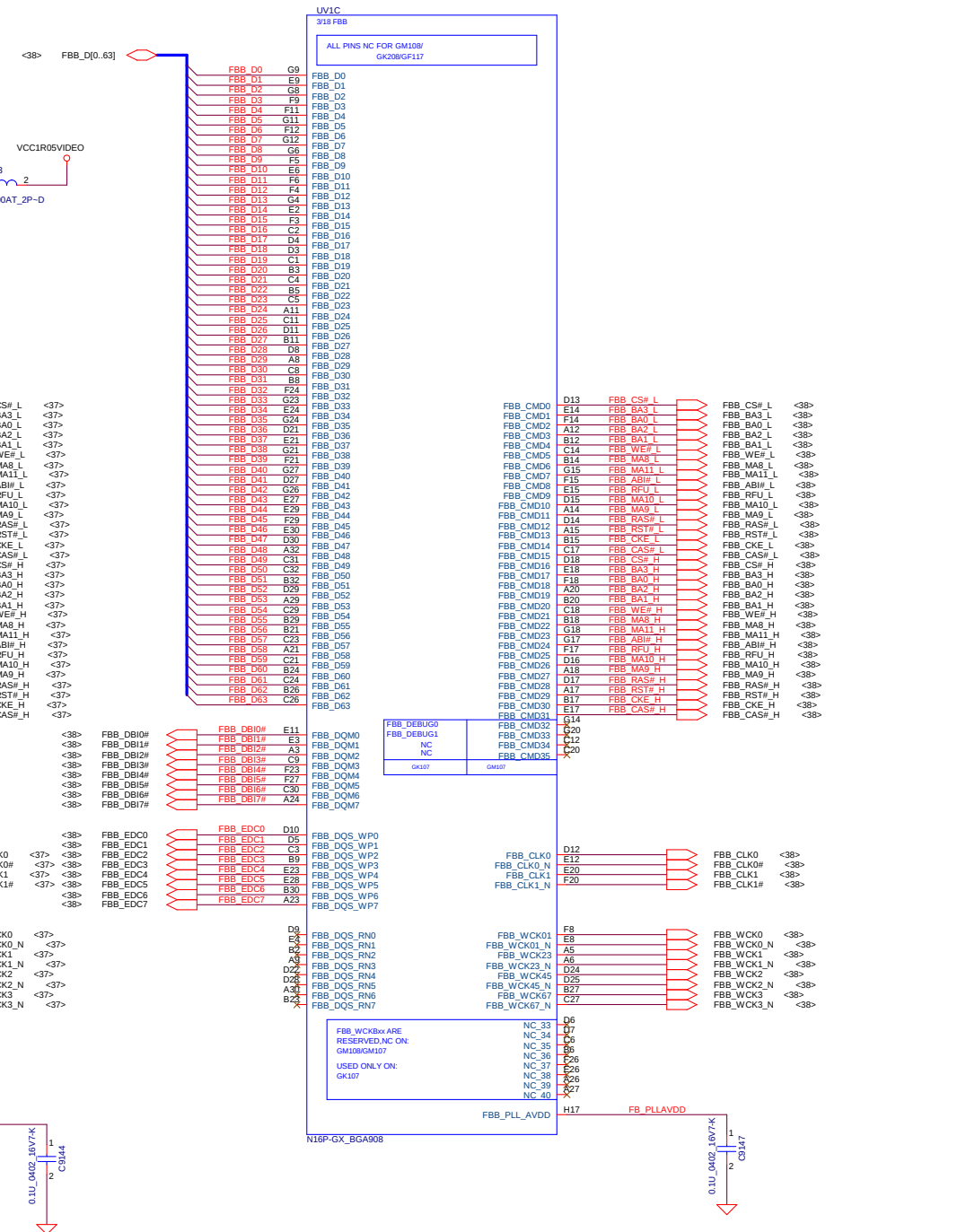
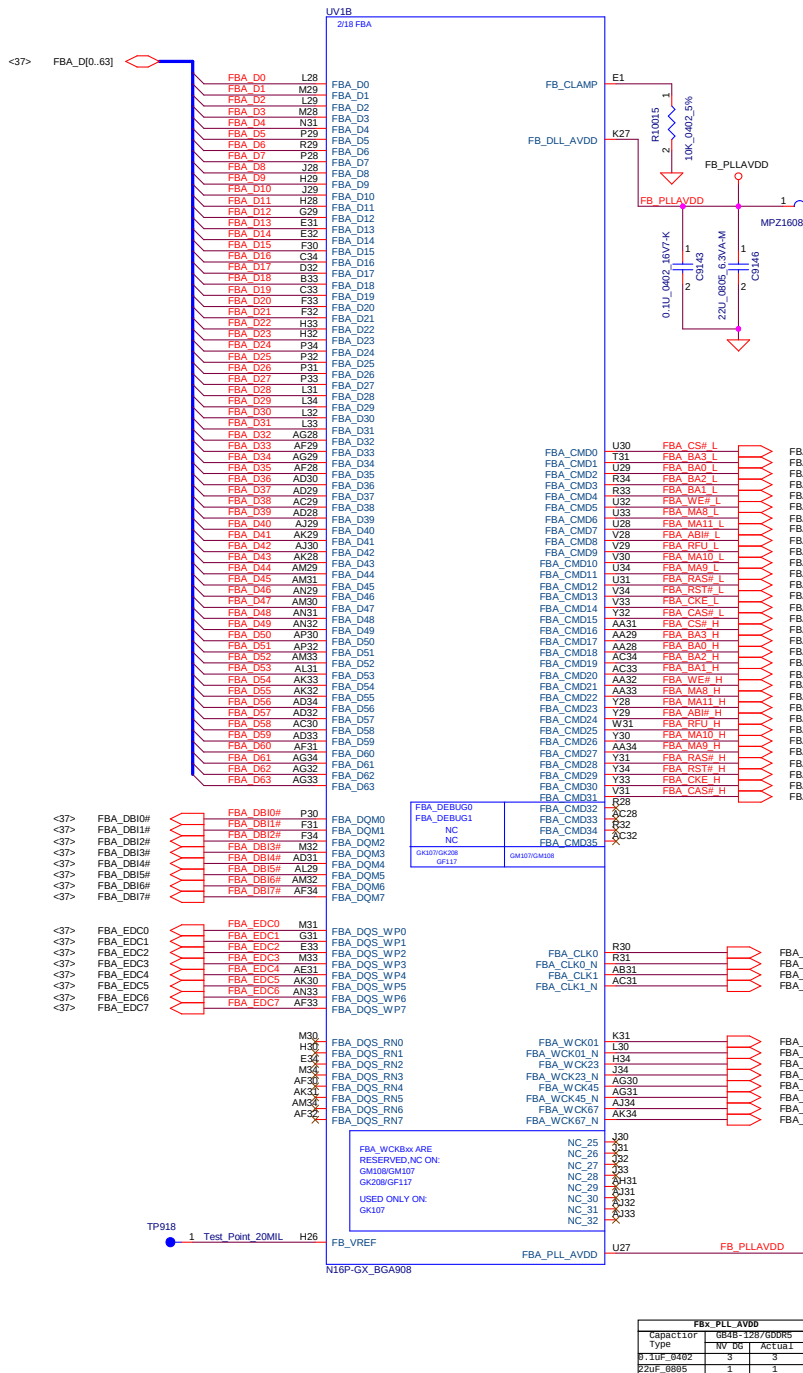
vinafix

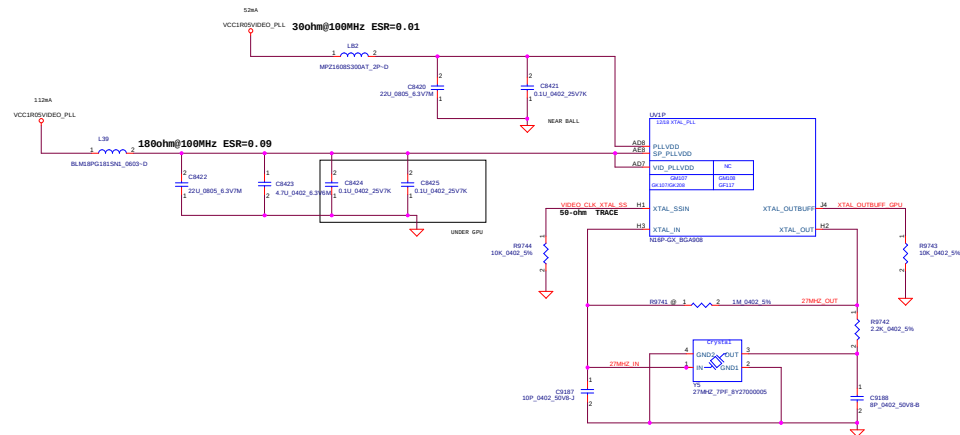
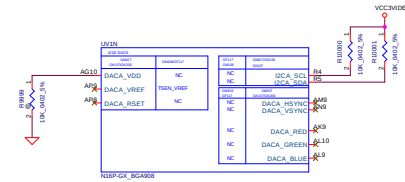
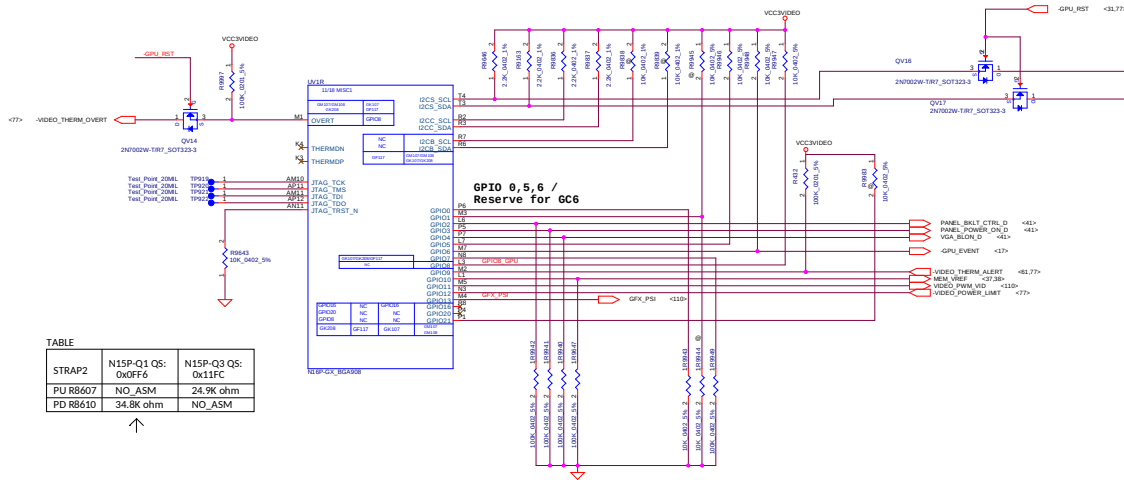




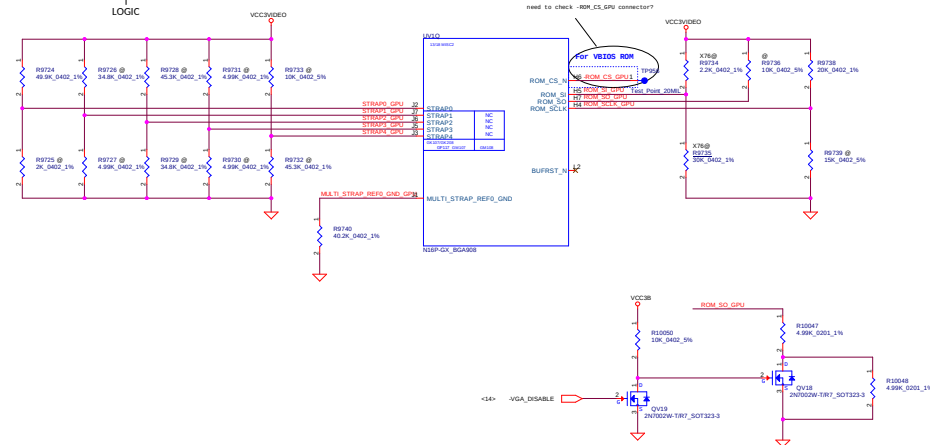


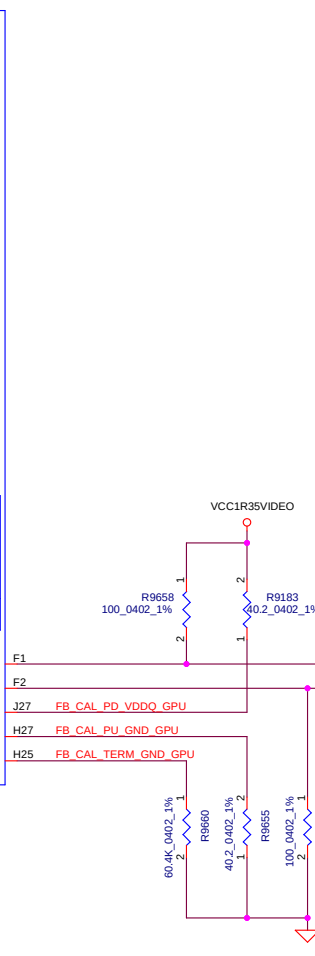
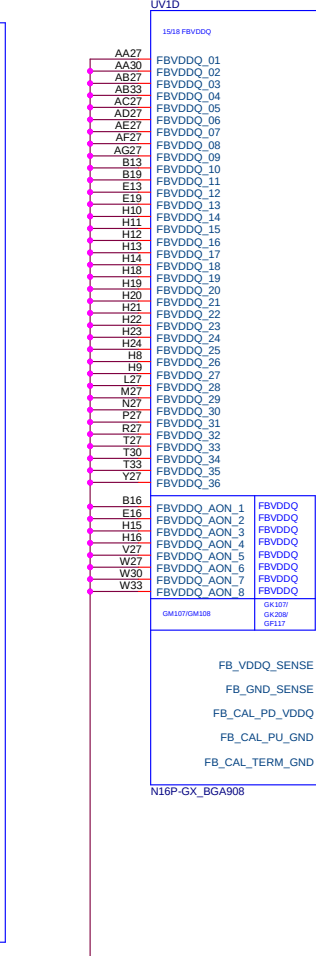
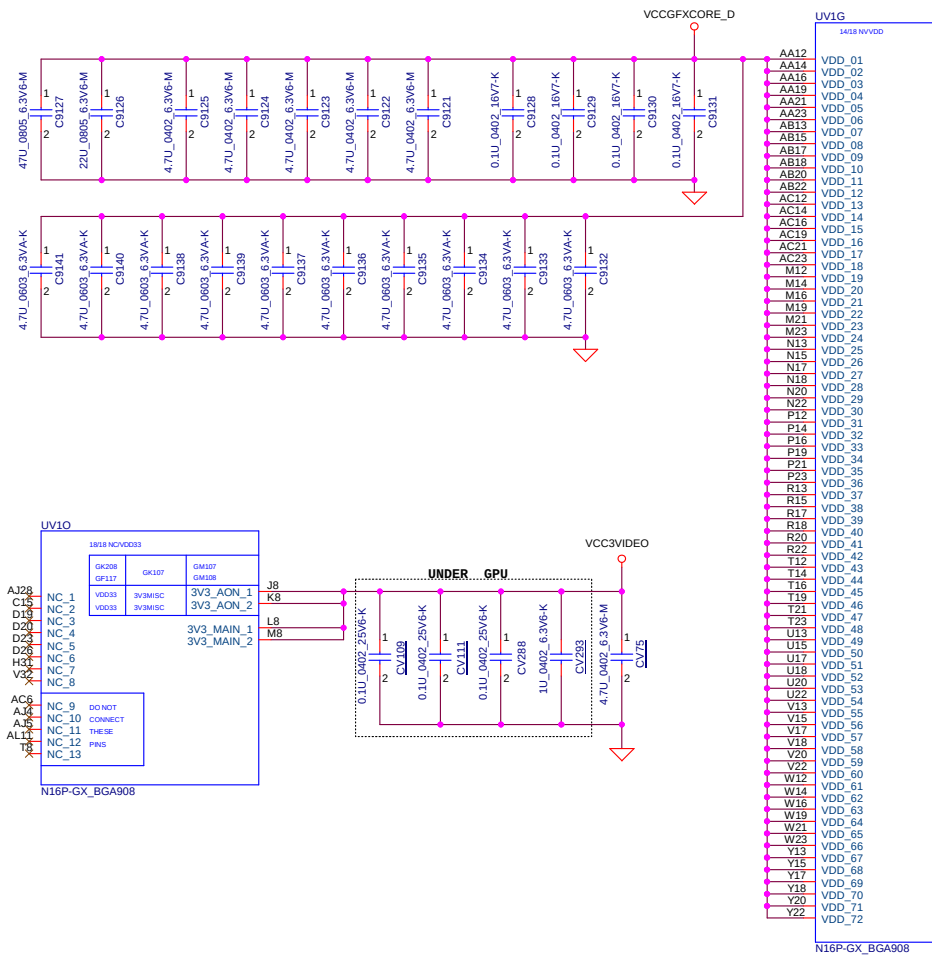
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		N16P-Q1/Q3(2/6): DIGITAL IC	
2015/07/16		2016/01/16		Rev 0.1	
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Sheet		32		of 118	

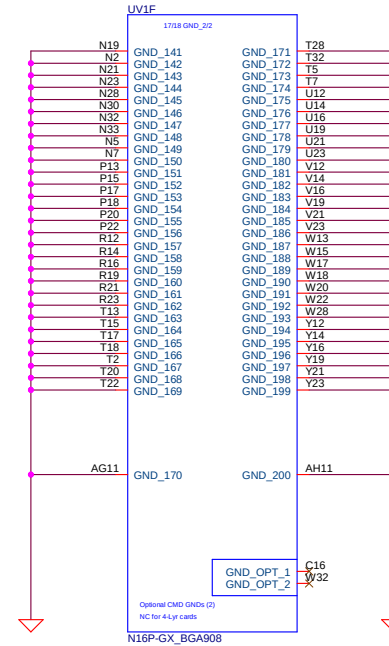
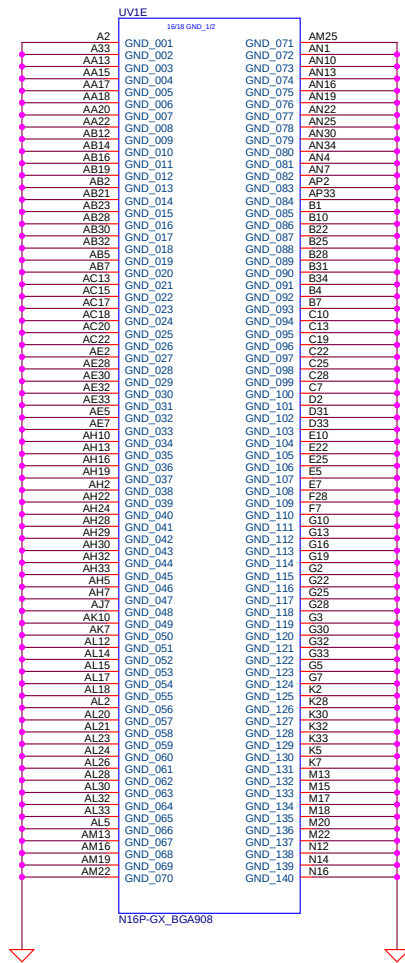




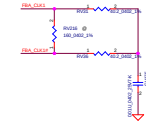
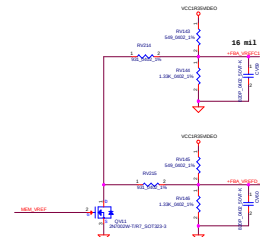
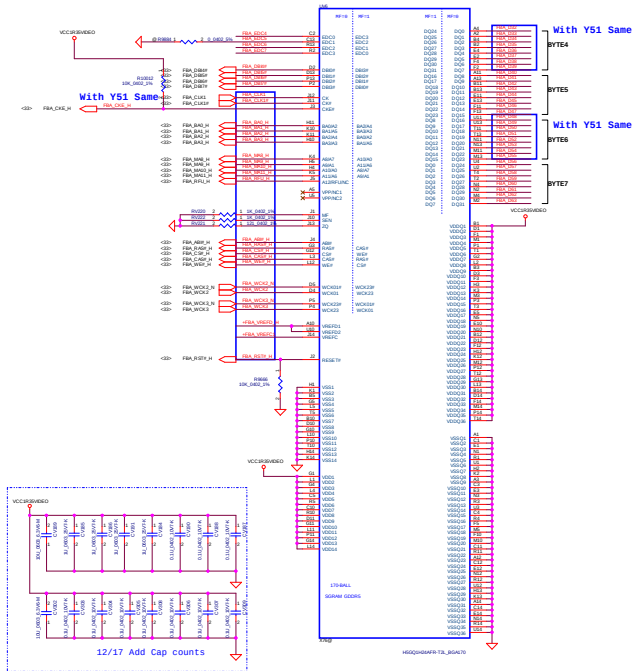
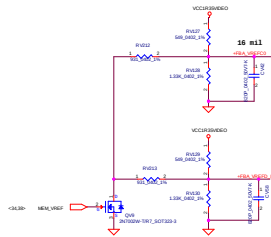
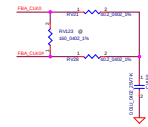
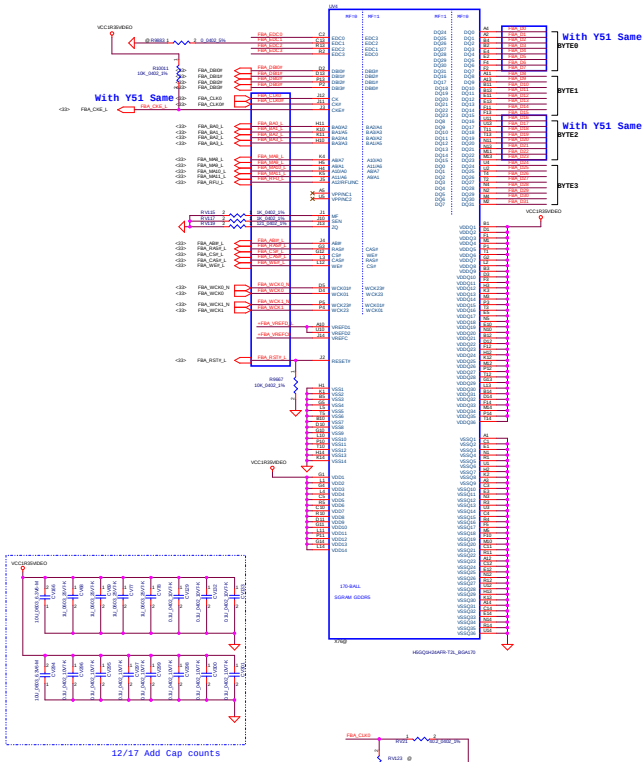
STRAP2	N16P-Q1 QS: 0x0FF6	N16P-Q3 QS: 0x11FC
PU R8607	NO_ASM	24.9K ohm
PD R8610	34.8K ohm	NO_ASM



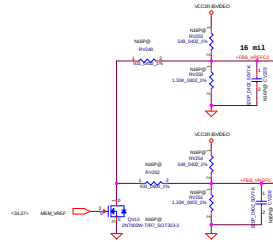
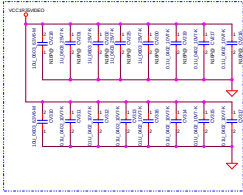





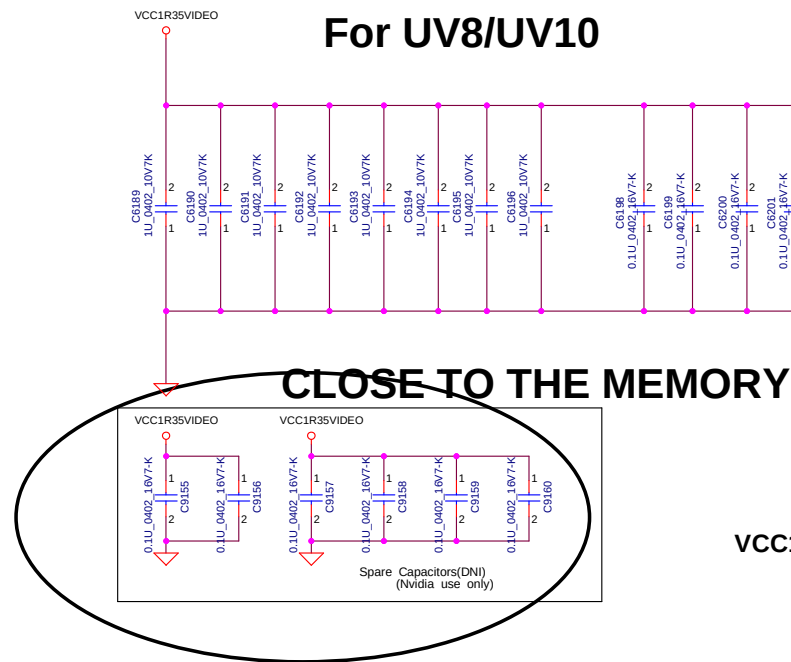
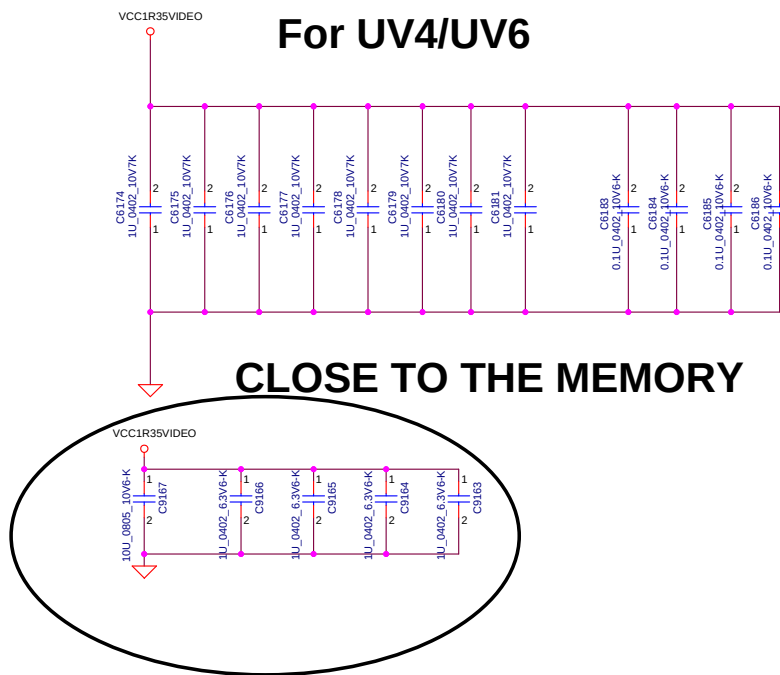
<3> FBA_DR_48
<3> FBA_DRQ2_48



Note: need to decide 4VRAM or 8VRAM before SDV design.



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Project Name Project No.				Project No. 01-118	




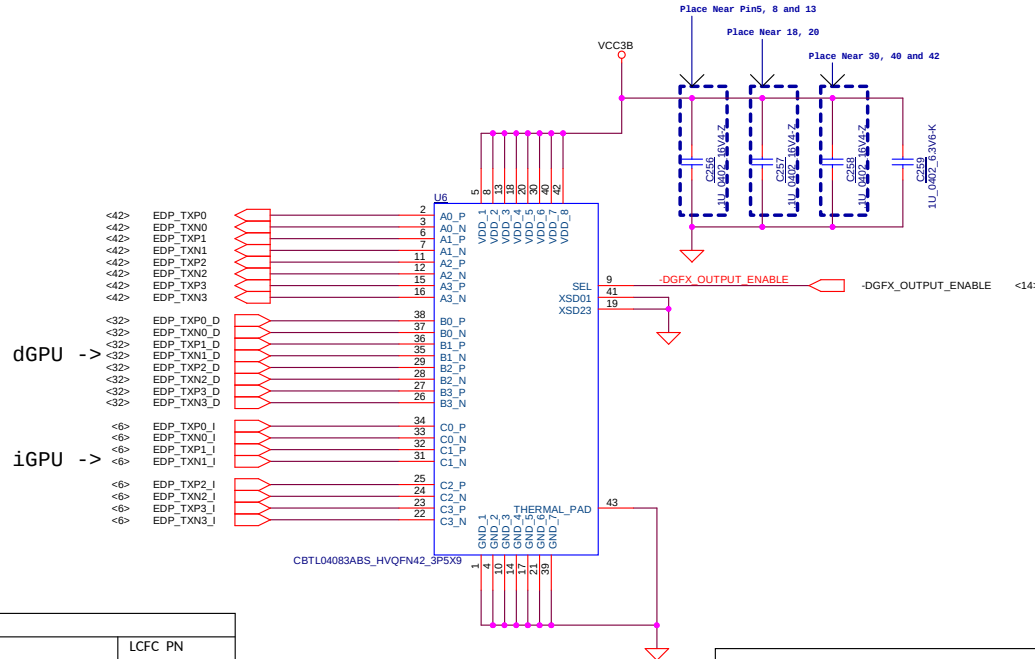
VCC1R35VIDEO Decaps:

1x 0805 10uF
6x 0402 0.1uF
4x 0603 1.0uF

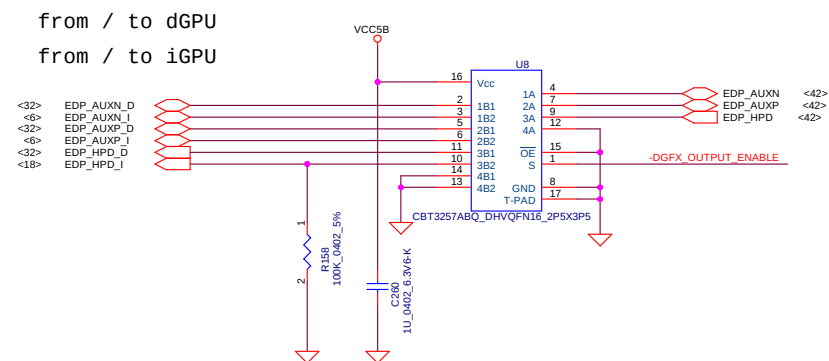
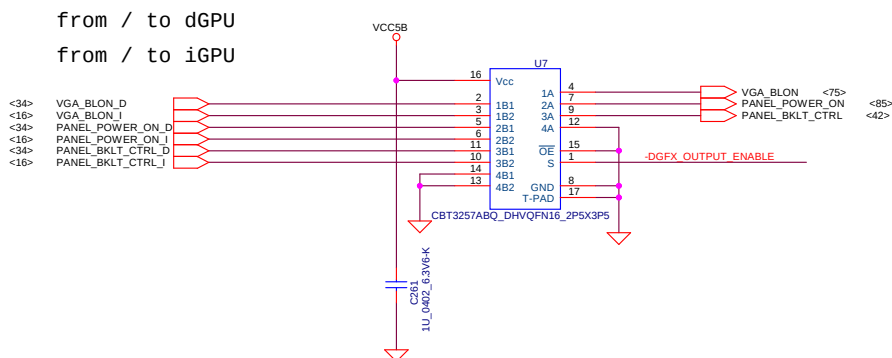
VCC1R35VIDEO Decaps:

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4x 0603 1.0uF

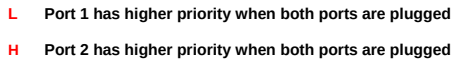
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DOCK DP Switch		
Vendor	Vendor PN	LCFC PN
NXP	CBTL04083ABS	
Pericom	PI3PCIE3412ZHE+DAX	

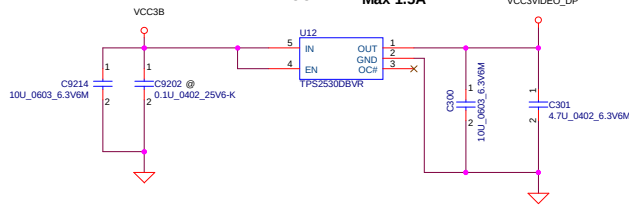


DP_DGL_DTCT	DP MODE	2SK3541	RTM002	AUXP/N
LOW	DP (Native)	OFF	OFF	No pull-up
HIGH	TMDS (Dongle)	ON	ON	Pull up to 4.7k

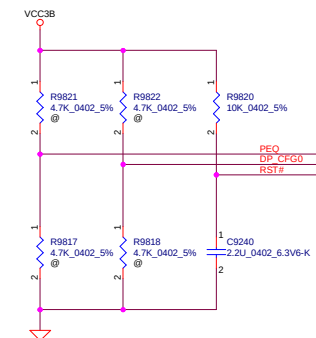
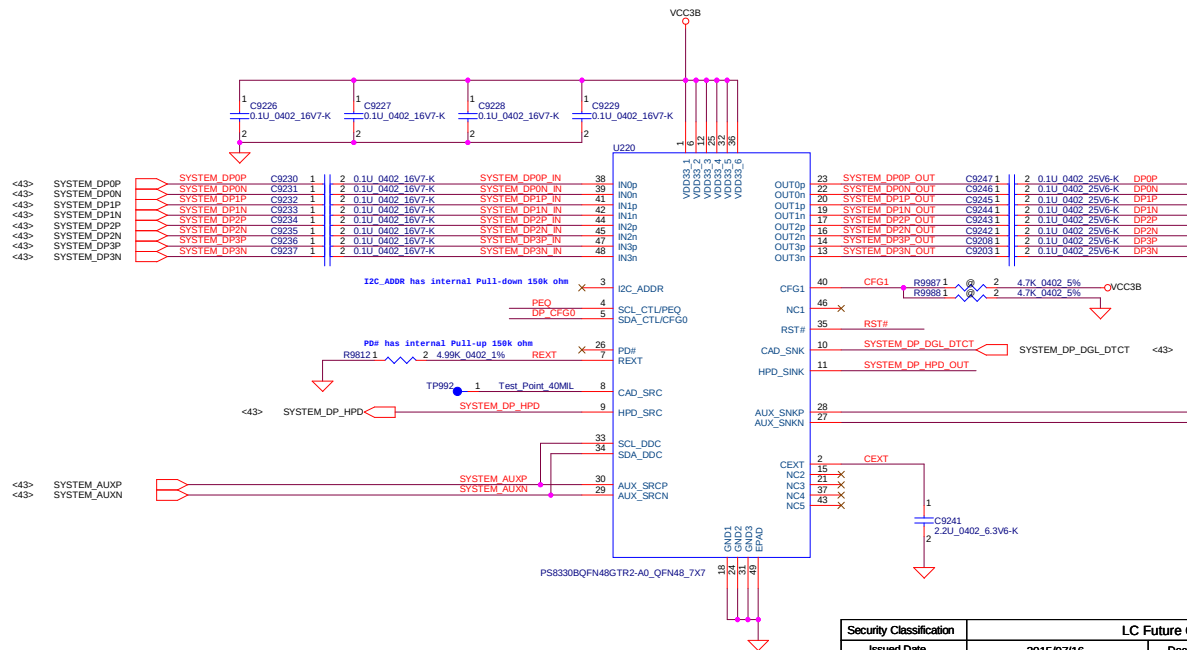
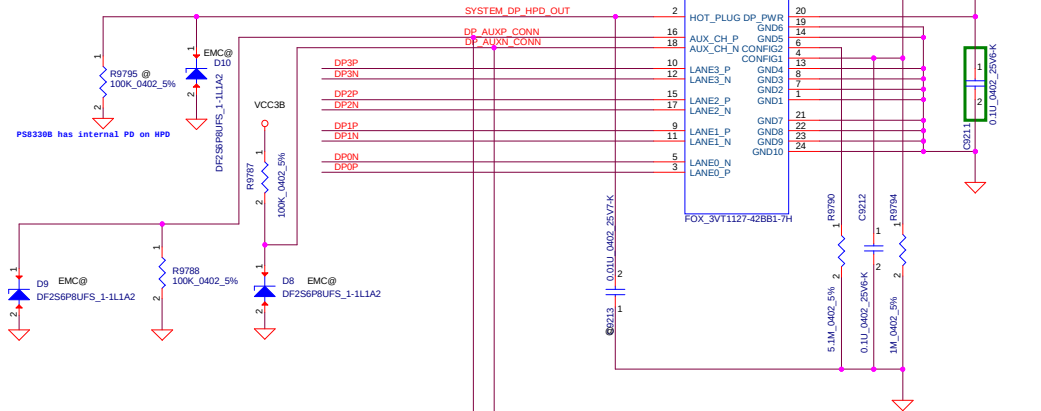
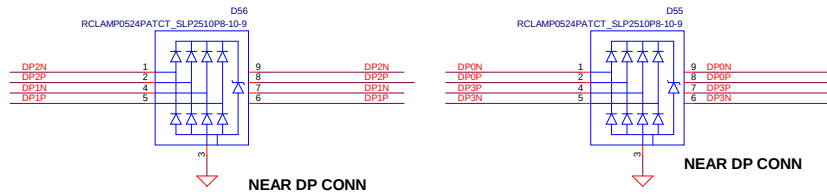


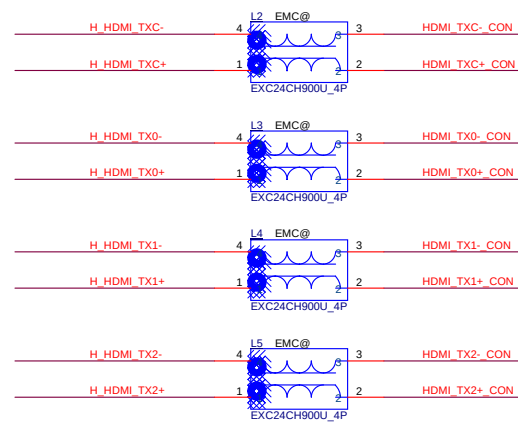
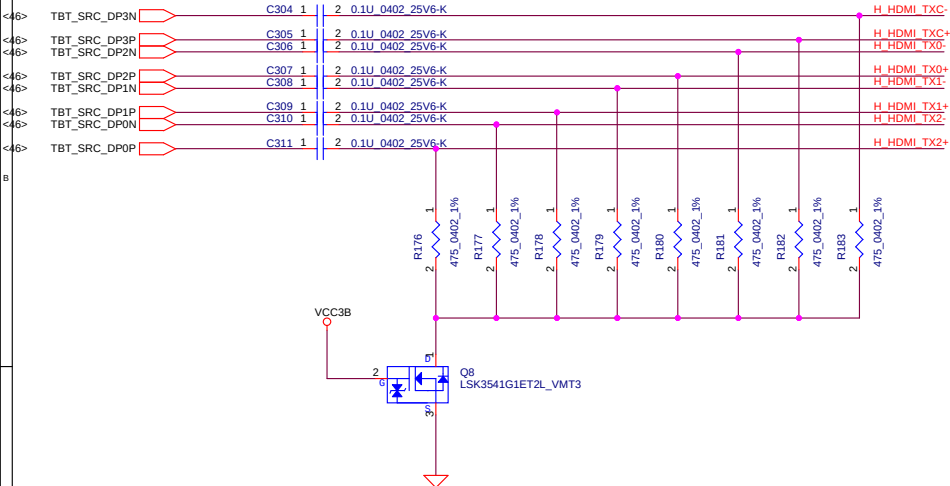
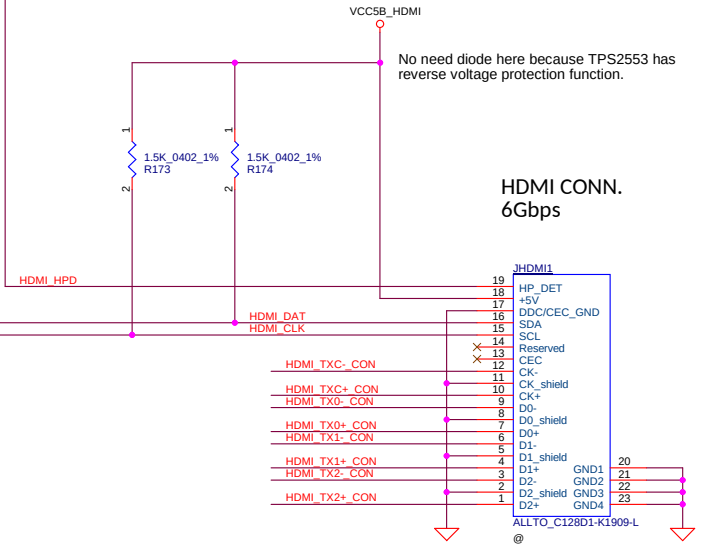
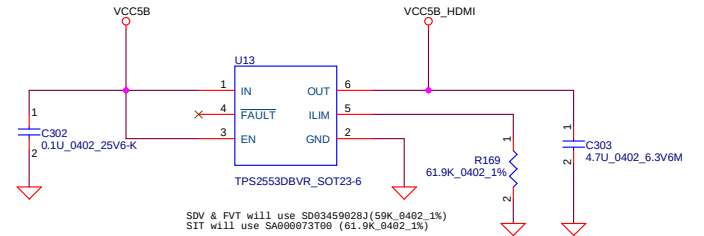
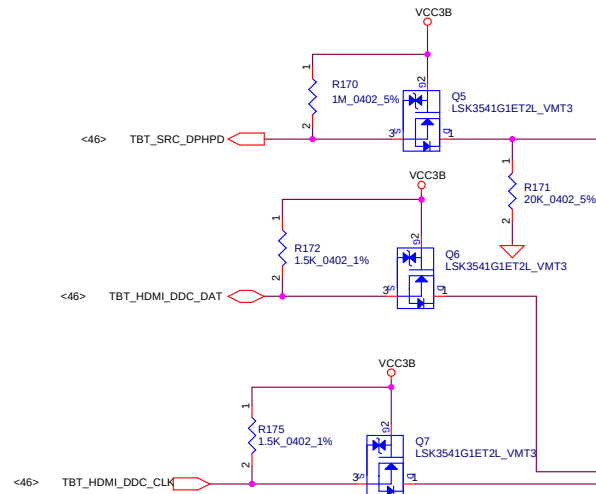
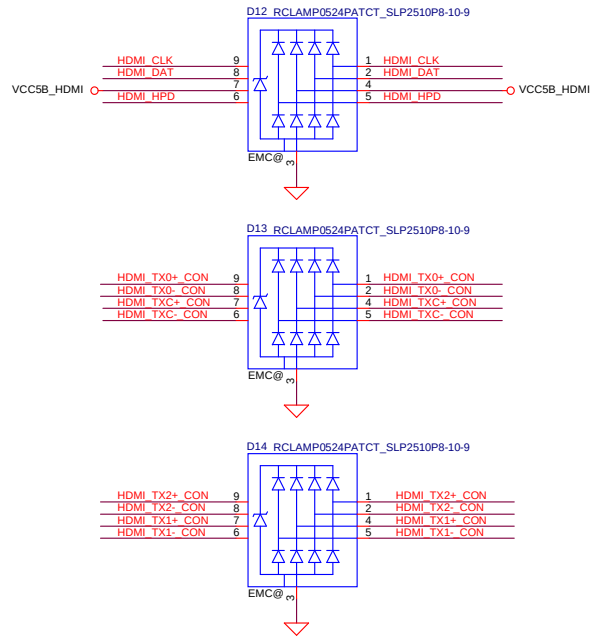
		Auto test	Input offset cancellation
CFG1	L	Disable	Enable
	H	Enable	Enable
	M	Disable	Disable


Title DP DEMUX			
Size Custom	Document Number NM-A451	Rev 0.1	
Date:	Friday, October 02, 2015	Sheet	43 of 116




Vendor	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G






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						Date:	Friday, October 02, 2015		Sheet 45 of 116


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				Custom	NM-A451		0.1
Date:				Friday, October 02, 2015		Sheet	48 of 116


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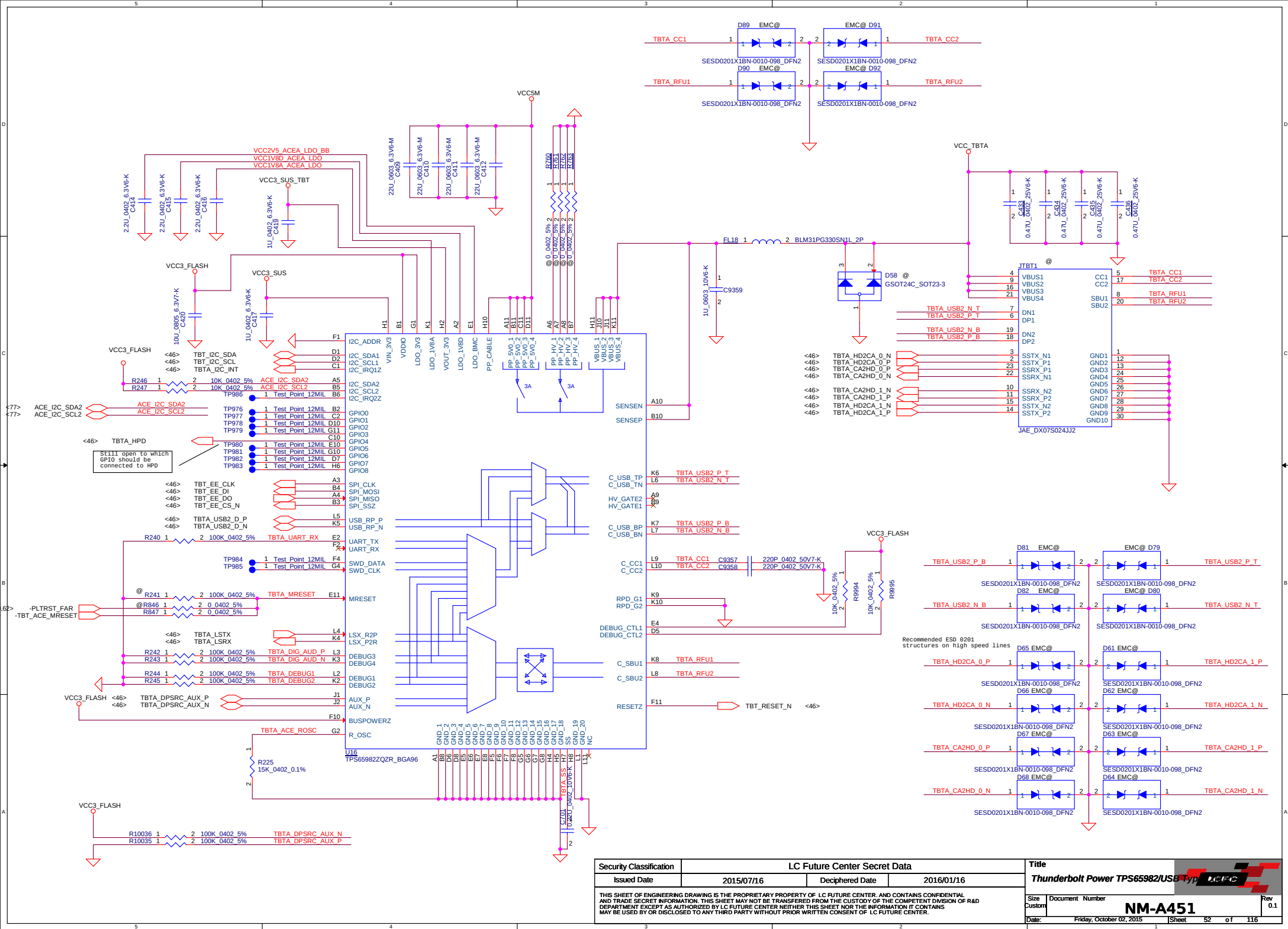
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				Custom	NM-A451	0.1	
Date:				Friday, October 02, 2015	Sheet	49 of 116	

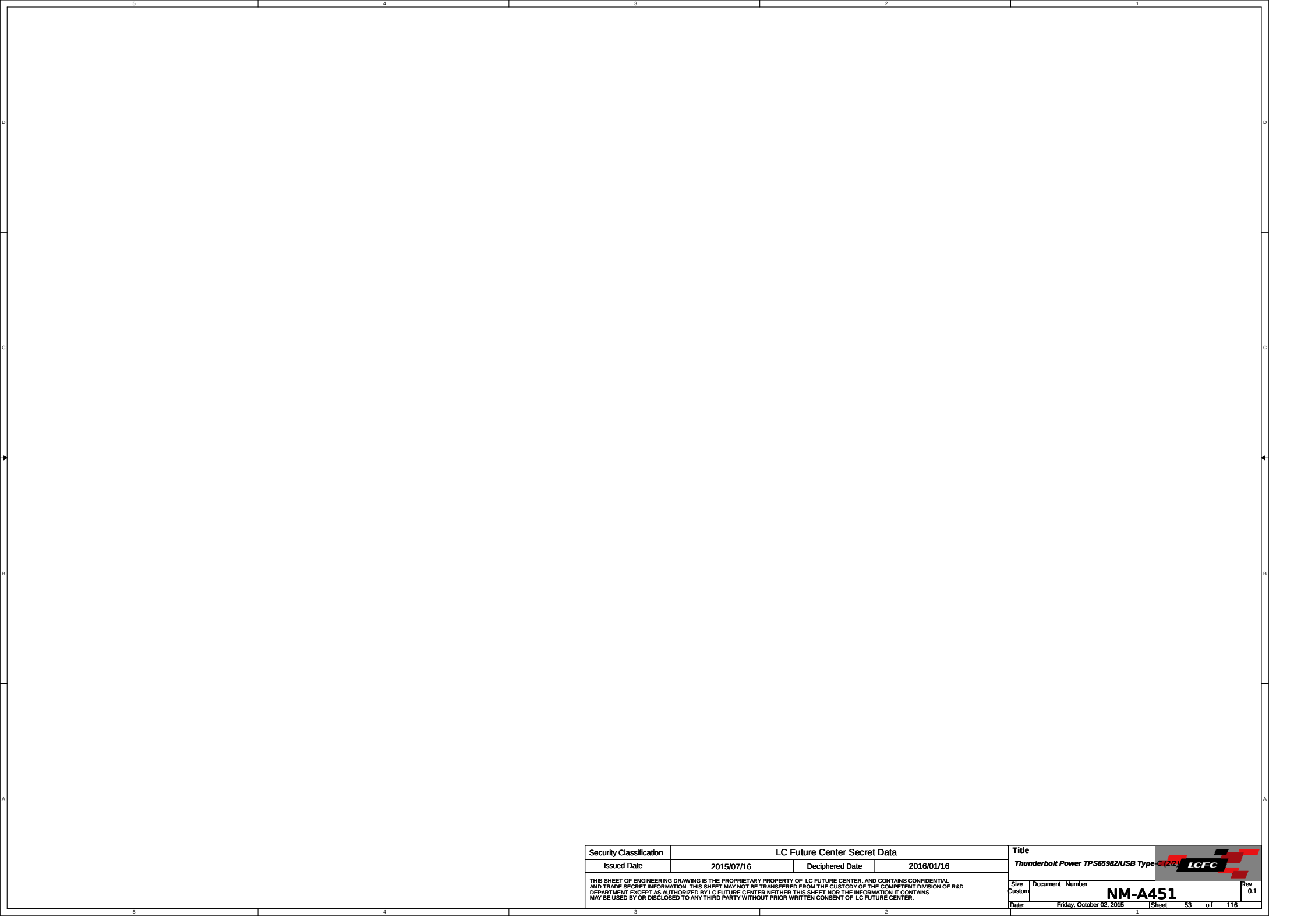
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				Date: Friday, October 02, 2015			Sheet 50 of 116

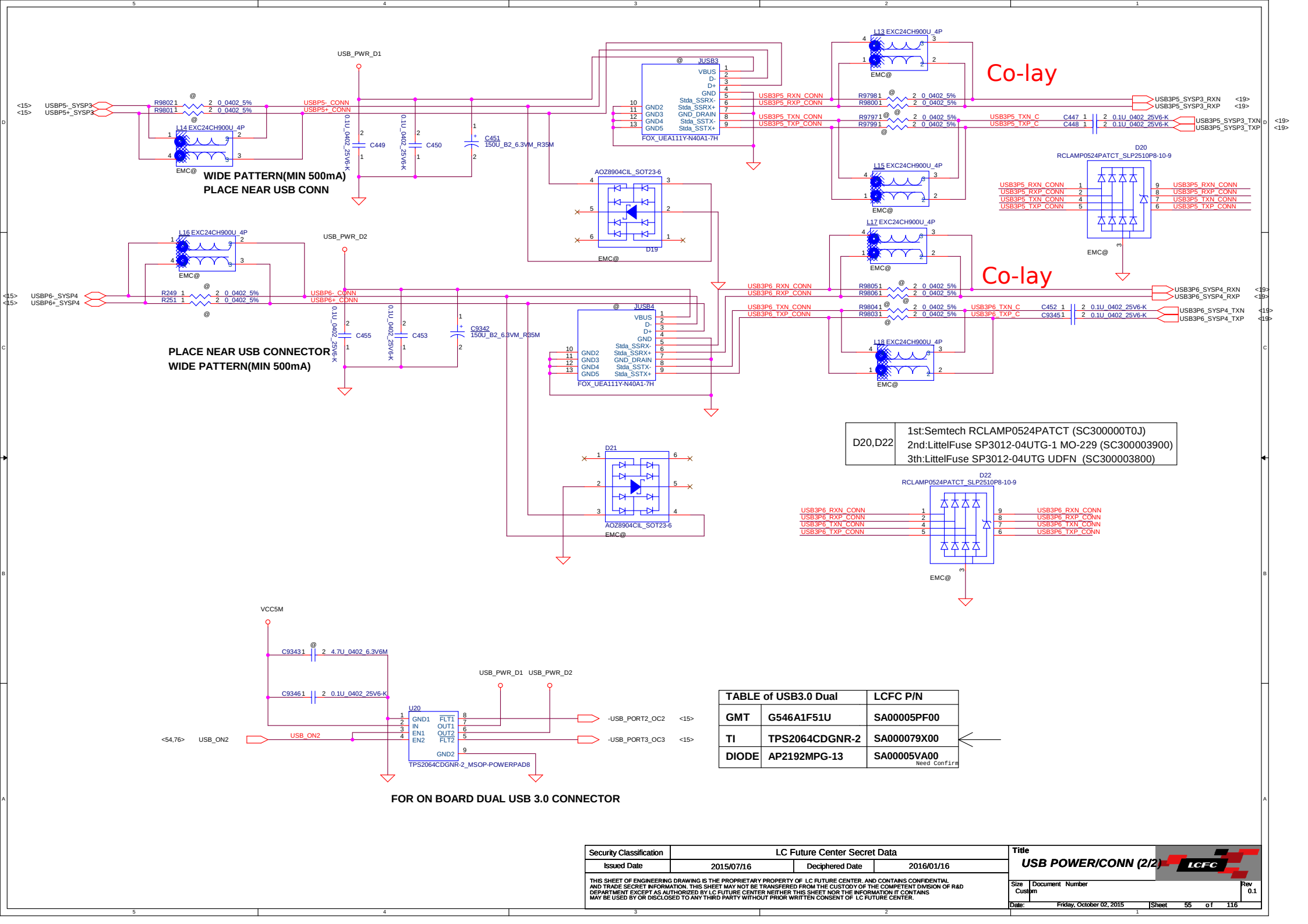
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Co-lay

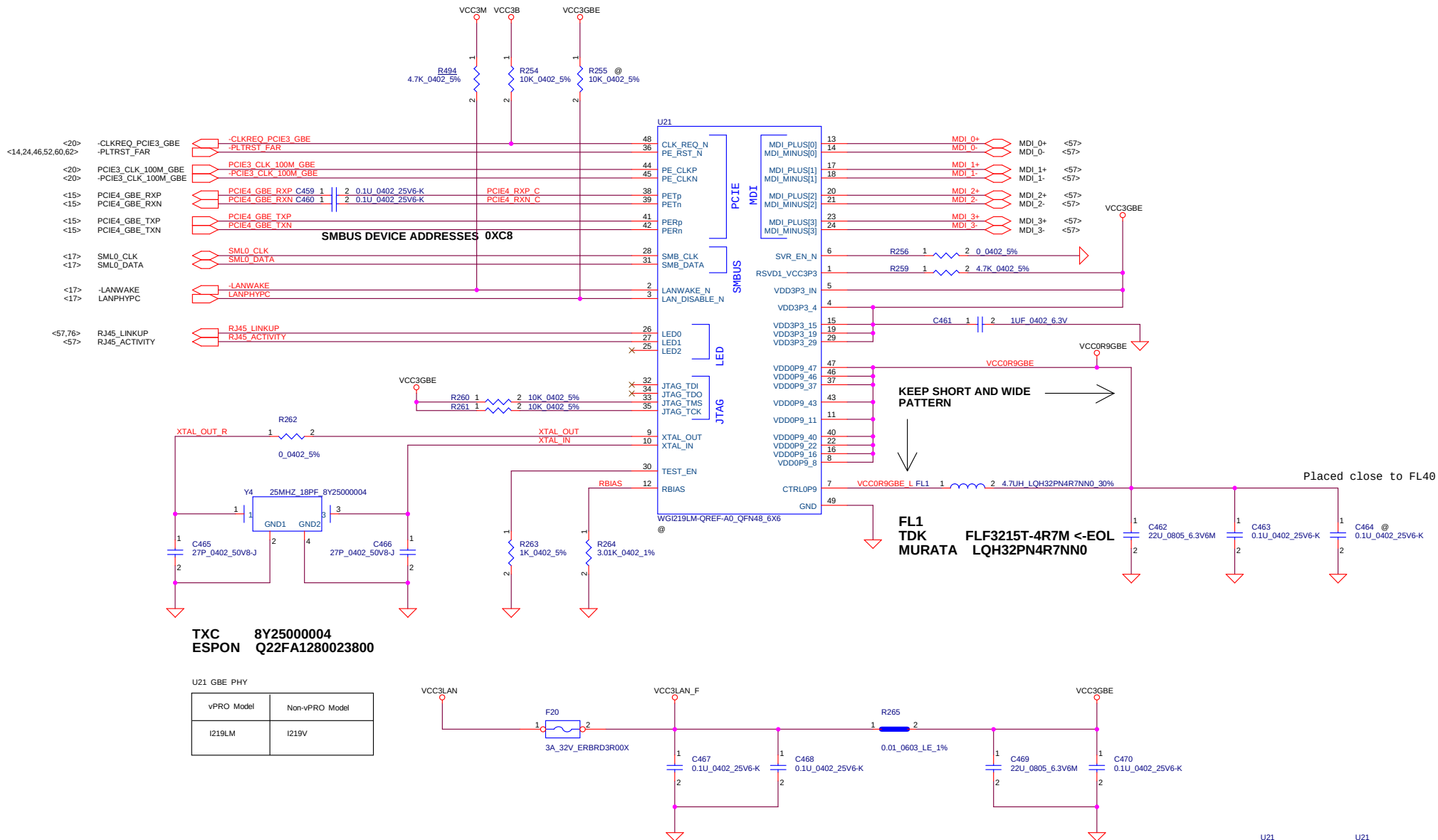
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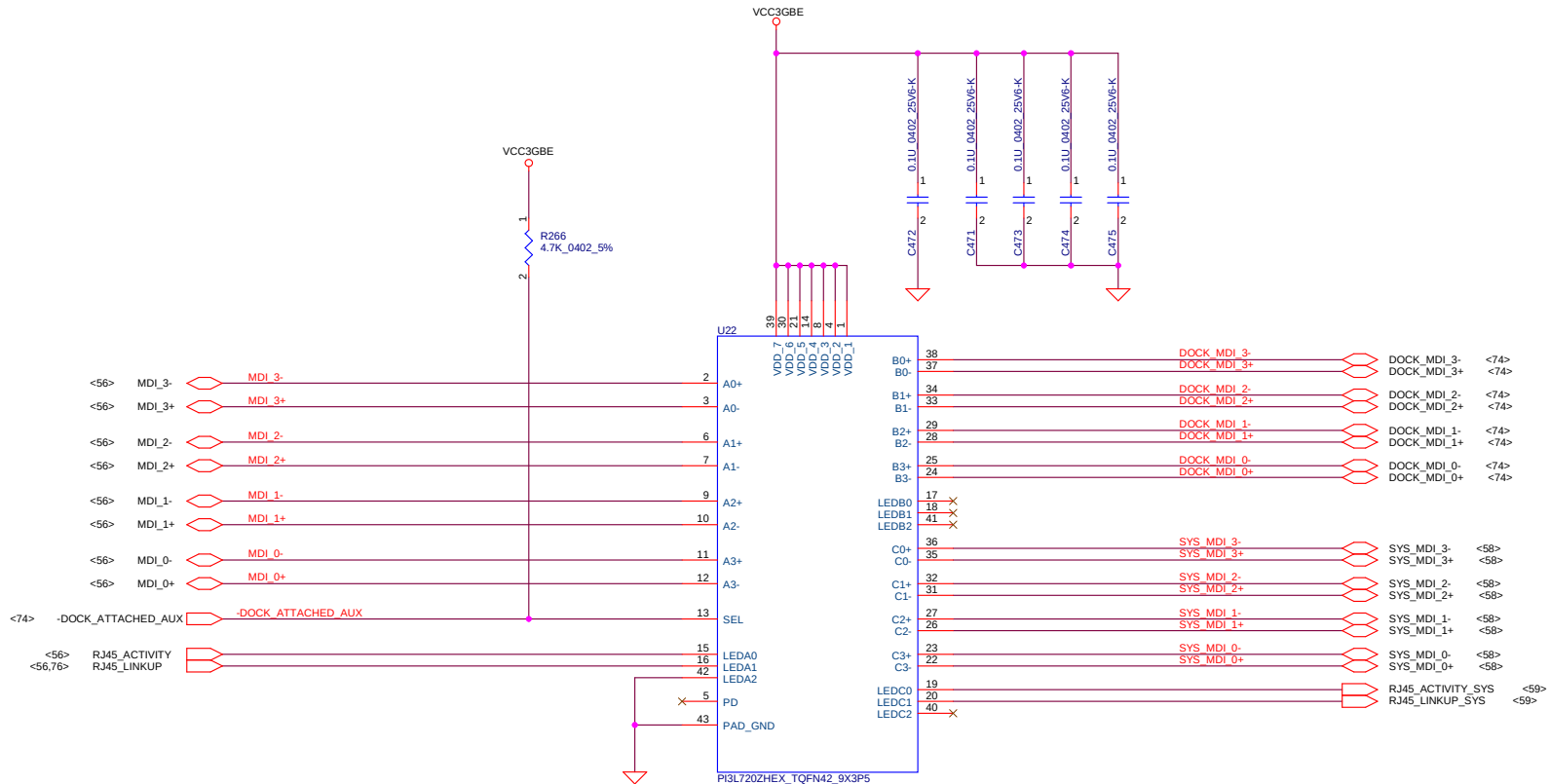
D20,D22	1st:Semtech RCLAMP0524PATCT (SC300000T0J)
	2nd:Littelfuse SP3012-04UTG-1 MO-229 (SC300003900)
	3th:Littelfuse SP3012-04UTG UDFN (SC300003800)

TABLE of USB3.0 Dual		LCFC P/N
GMT	G546A1F51U	SA00005PF00
TI	TPS2064CDGNR-2	SA000079X00
DIODE	AP2192MPG-13	SA00005VA00 Need Confirm

Security Classification		LC Future Center Secret Data	
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Title				USB POWER/CONN (2/2)				LCFC			
Size		Document Number		Rev		Date		Friday, October 02, 2015		Sheet 55 of 116	






THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

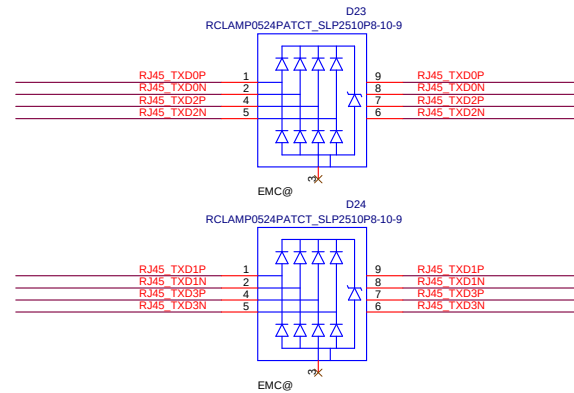
C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

ESD REASON

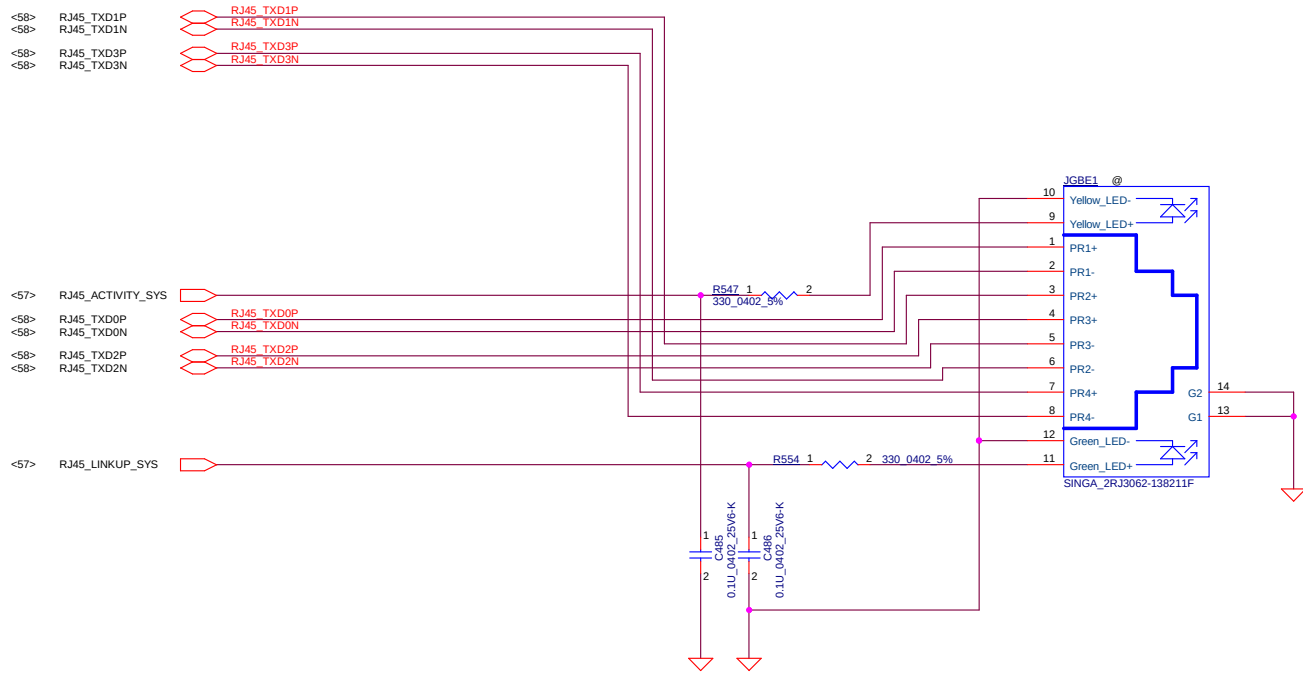
T1

Vendor	P/N
Timag	IH-115-F
Bothhand	NA69LF

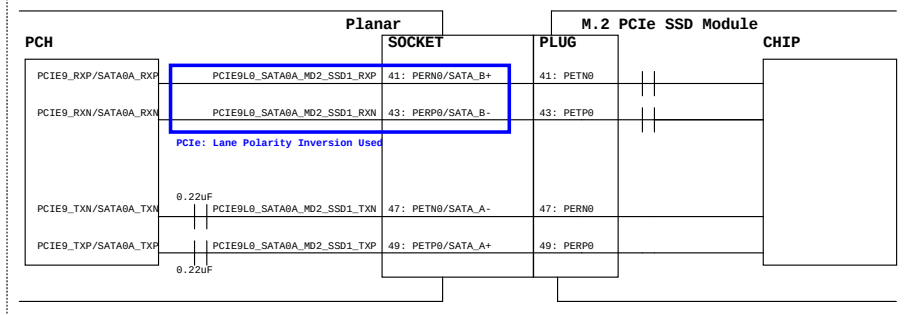
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Issued Date	2015/07/16	Deciphered Date	2016/01/16	GBE MAGNETICS				
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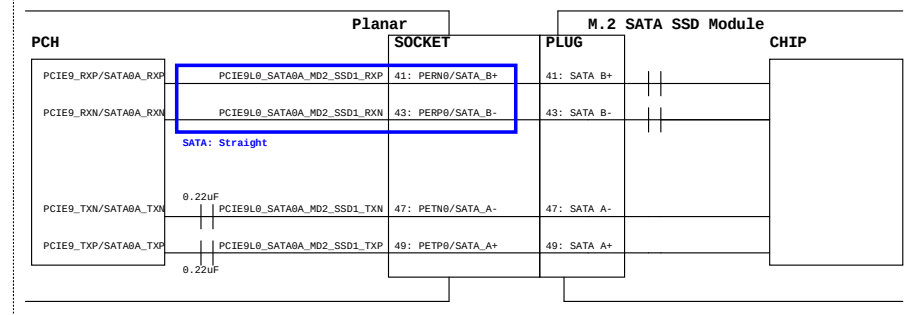
- | | |
|---------|--|
| D23,D24 | 1st:Semtech RCLAMP0524PATCT (SC300000T0J) |
| | 2nd:LittelFuse SP3012-04UTG-1 MO-229 (SC300003900) |
| | 3th:LittelFuse SP3012-04UTG UDFN (SC300003800) |



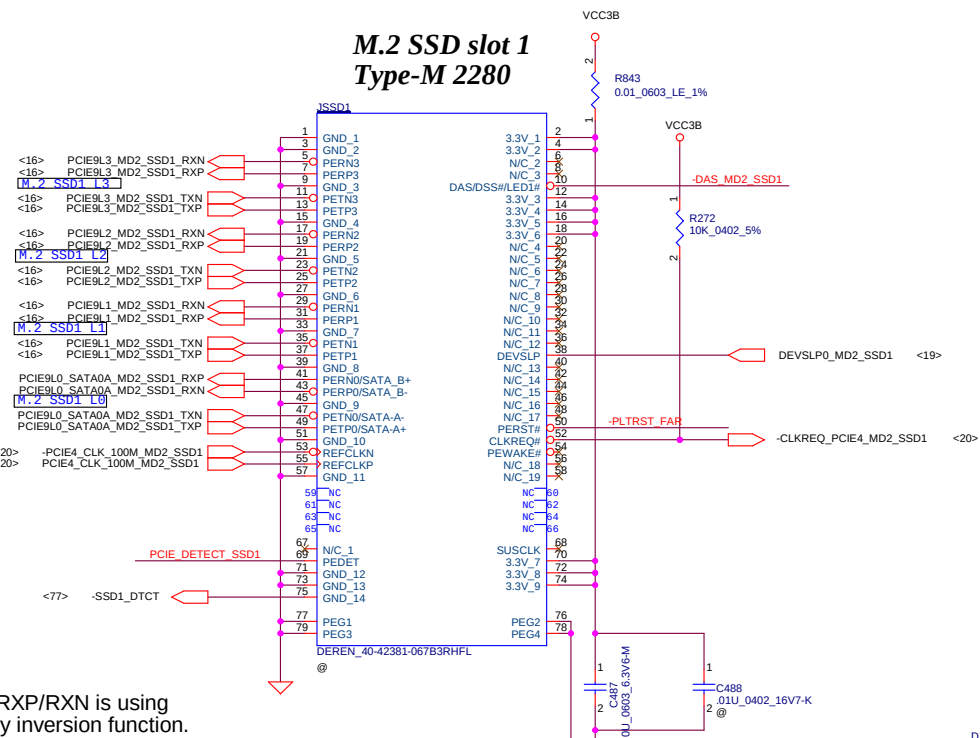
M.2 PCIe SSD



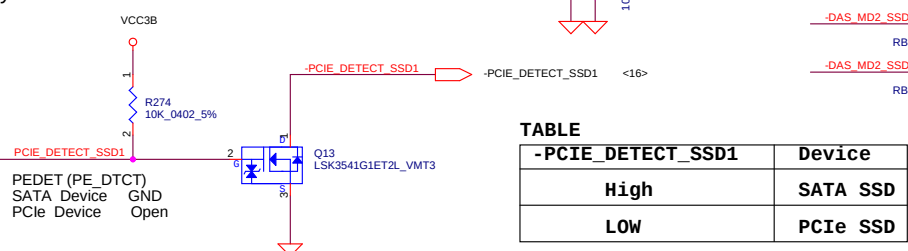
M.2 SATA SSD



M.2 SSD slot 1 Type-M 2280



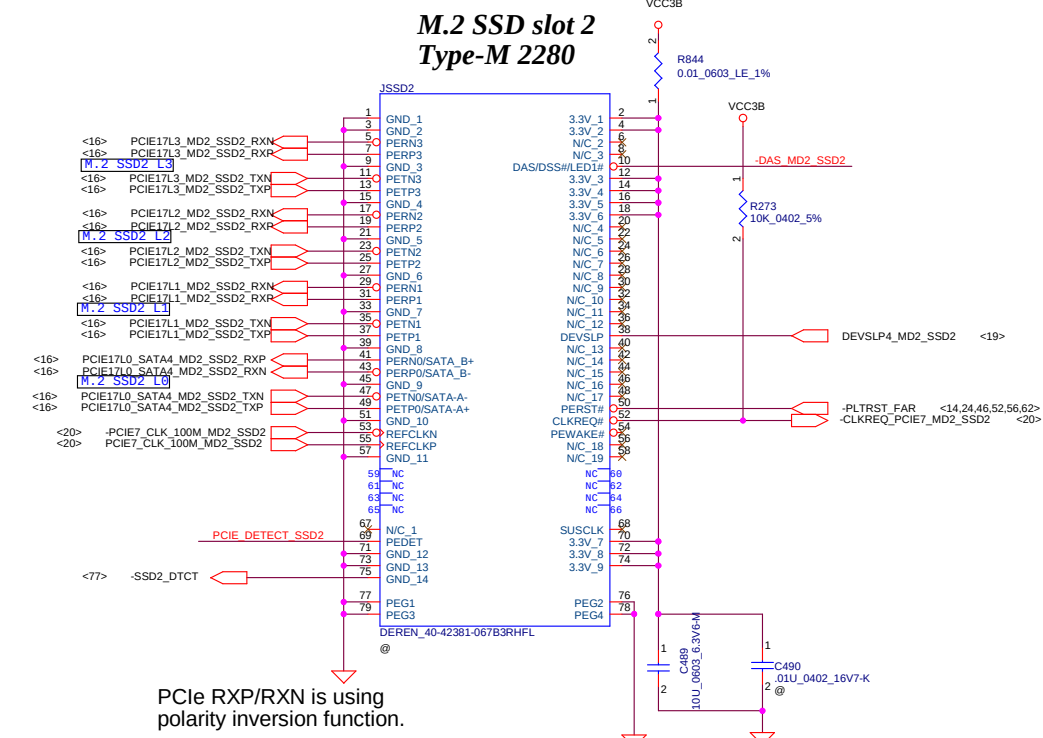
PCIe RXP/RXN is using polarity inversion function.



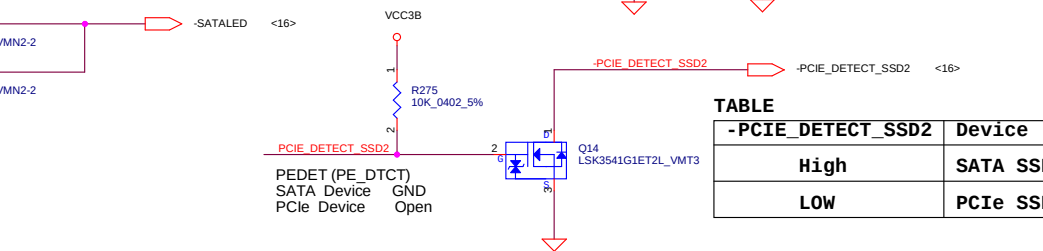
TABLE

-PCIE_DETECT_SSD1	Device
High	SATA SSD
Low	PCIe SSD

M.2 SSD slot 2 Type-M 2280



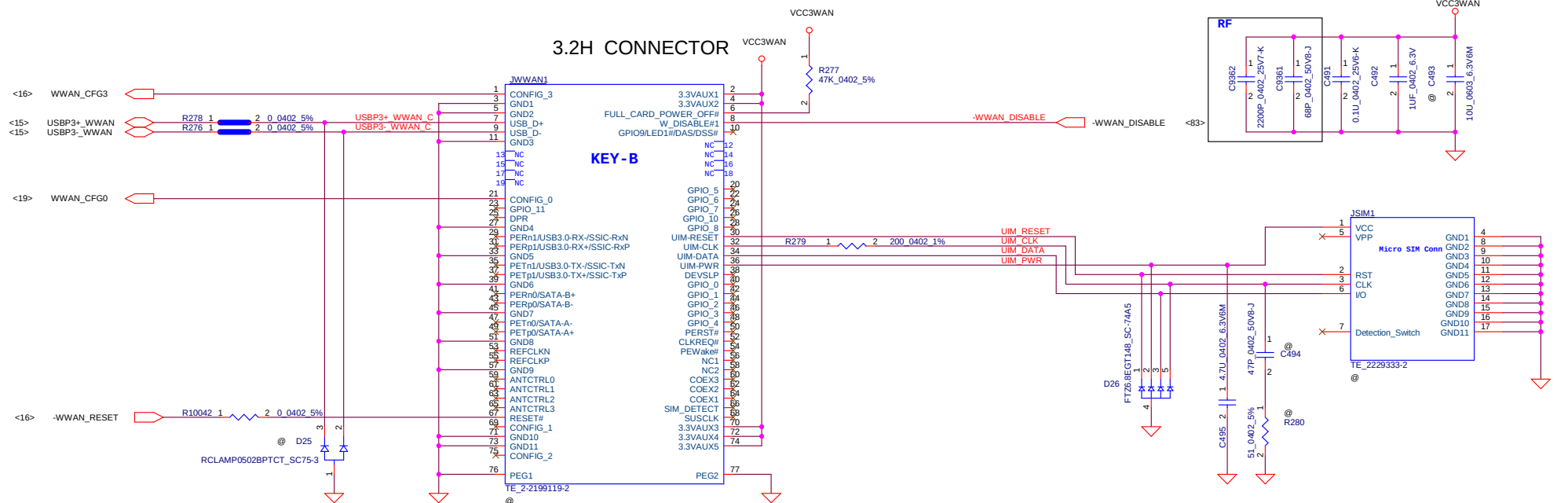
PCIe RXP/RXN is using polarity inversion function.



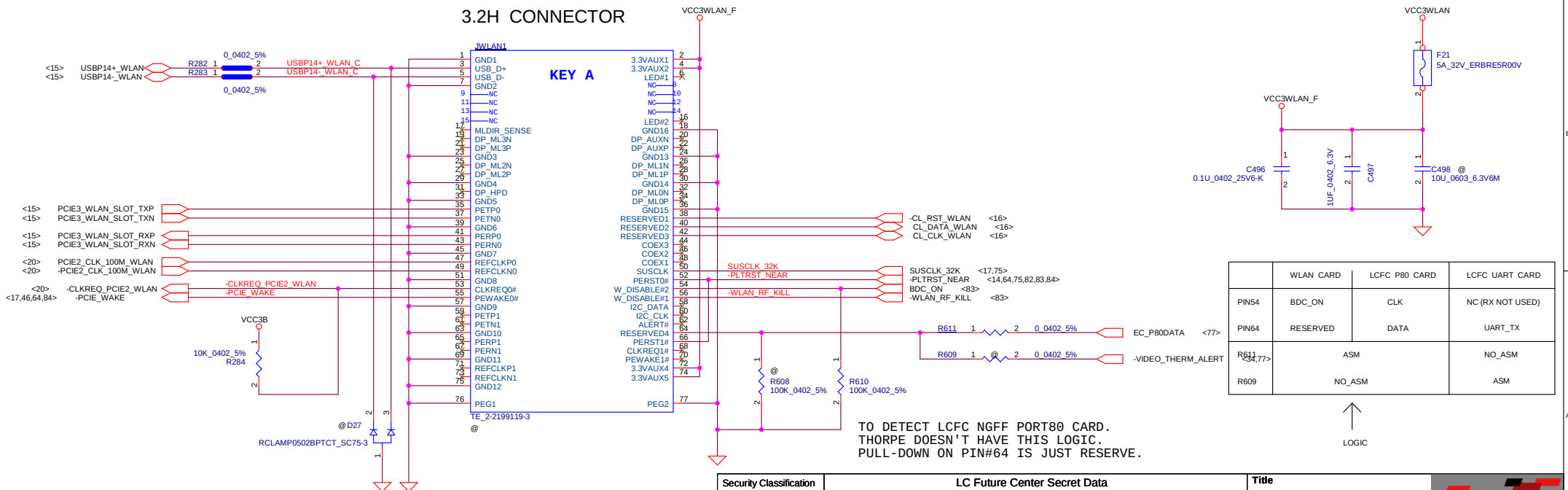
TABLE

-PCIE_DETECT_SSD2	Device
High	SATA SSD
Low	PCIe SSD

TYPE-B NGFF CCARD FOR WWAN




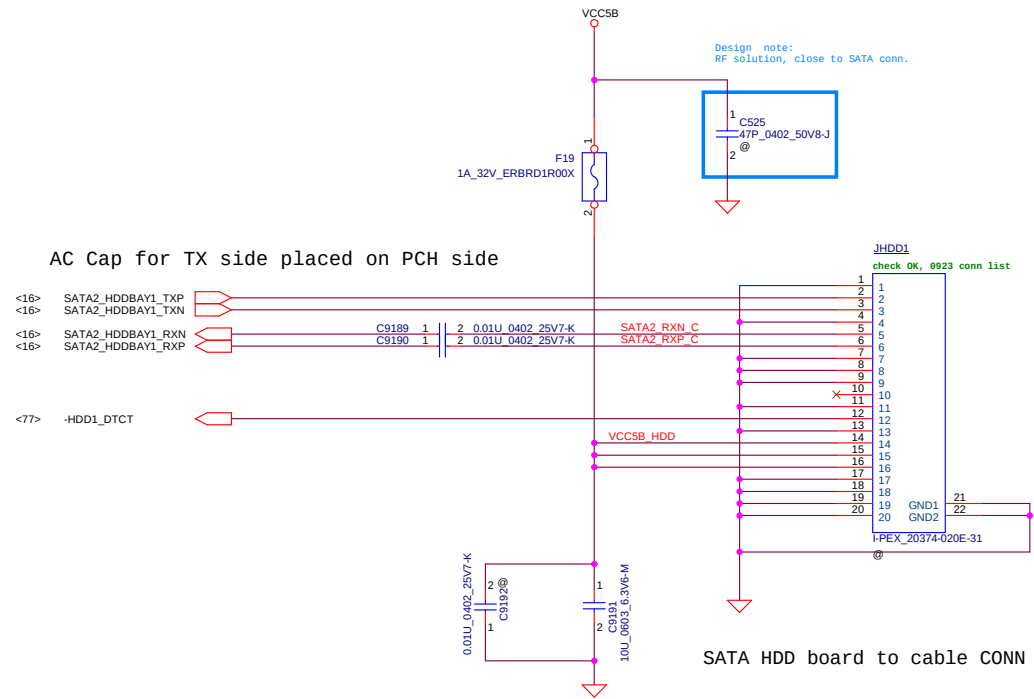
TYPE-A NGFF CCARD FOR WLAN



	WLAN_CARD	LCFC_P80_CARD	LCFC_UART_CARD
PIN54	BDC_ON	CLK	NC (RX NOT USED)
PIN64	RESERVED	DATA	UART_TX
R611 <34,77>	ASM		NO_ASM
R609	NO_ASM		ASM

TO DETECT LCFC NGFF PORT80 CARD.
THORPE DOESN'T HAVE THIS LOGIC.
PULL-DOWN ON PIN#64 IS JUST RESERVE.

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					NM-A451	0.1
				Date:	Friday, October 02, 2015	Sheet 61 of 116

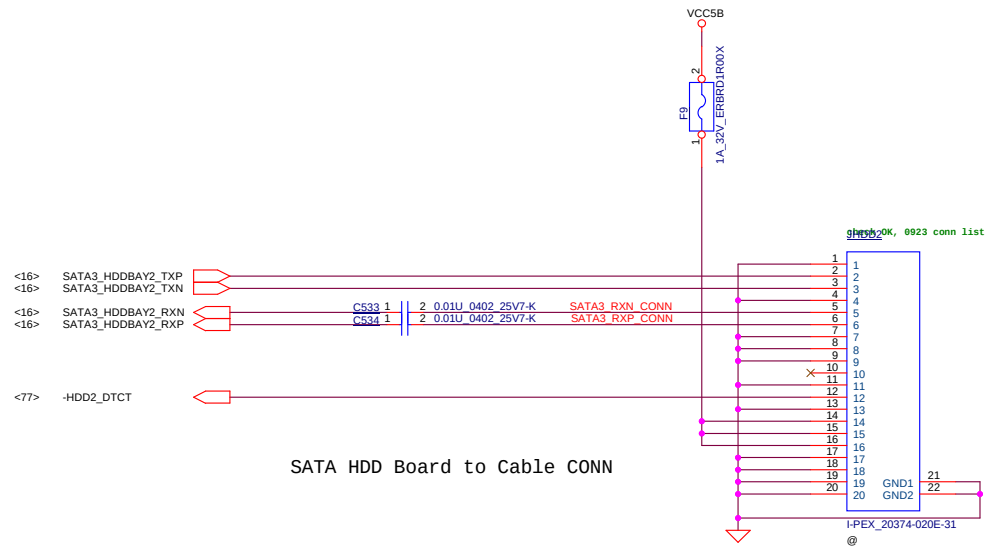
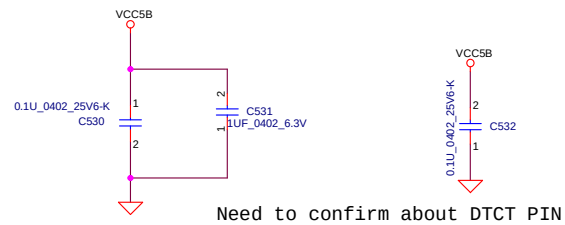


AC Cap for TX side placed on PCH side

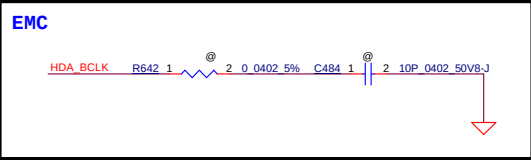
Design note:
RF solution, close to SATA conn.

JHDD1
check OK, 0923 conn list

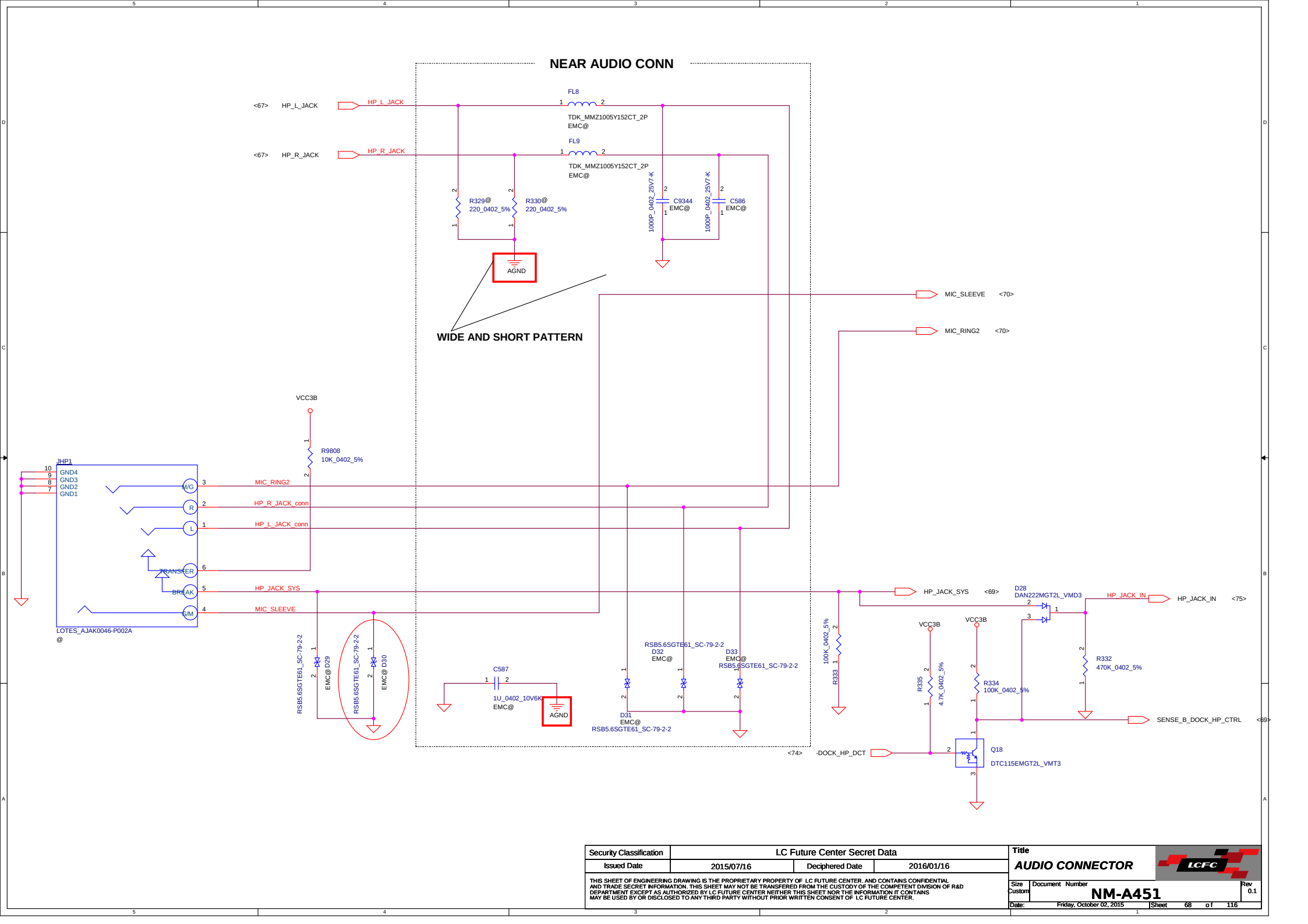
SATA HDD board to cable CONN

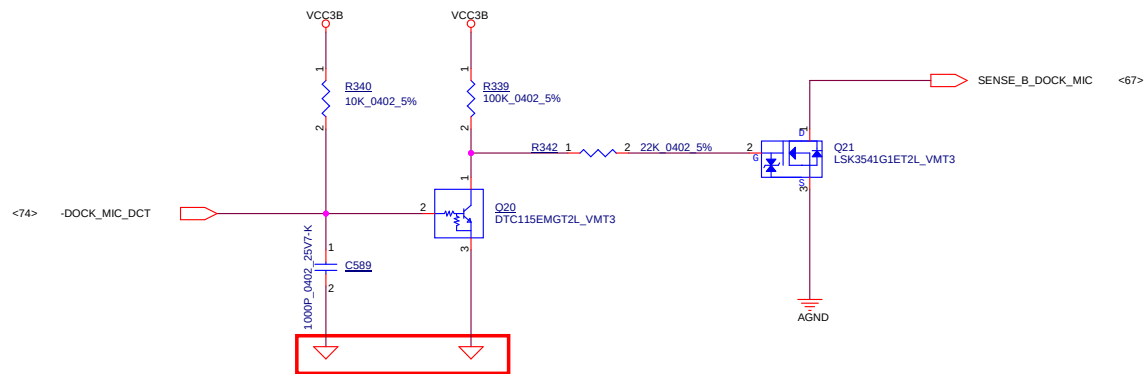
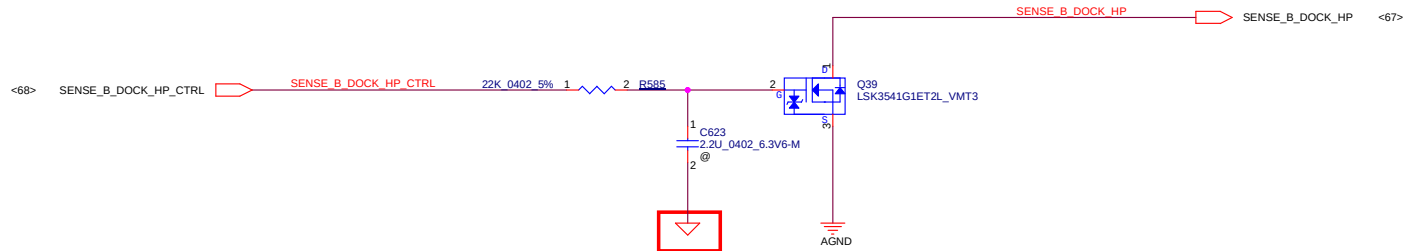
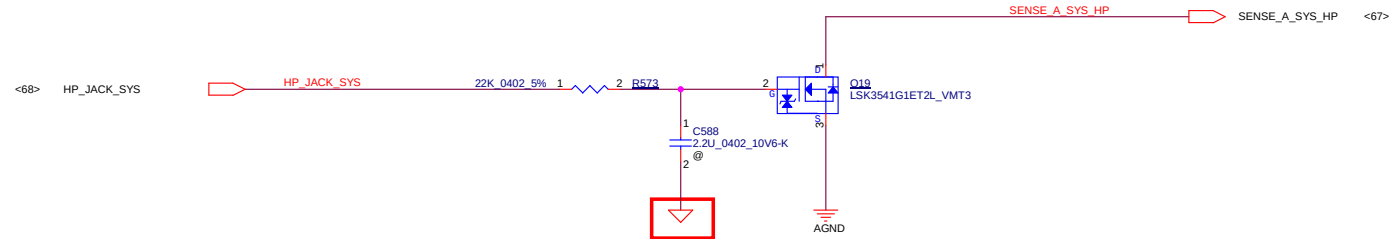


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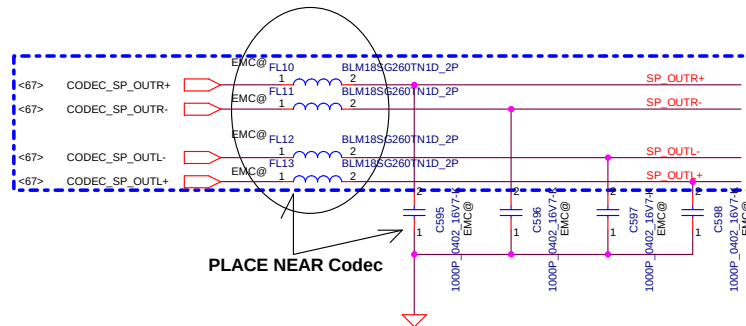




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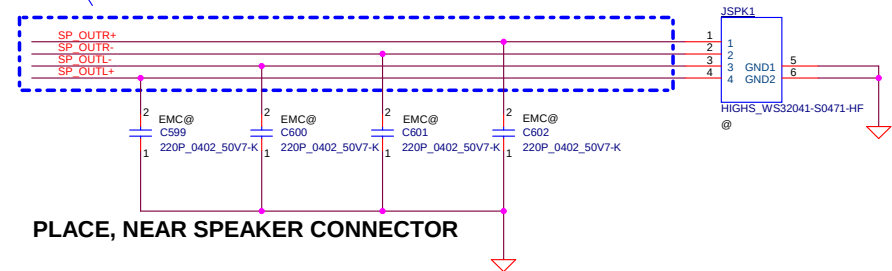
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Size	Document Number	NM-A451		Rev	0.1
Date:	Friday, October 02, 2015	Sheet	69	of	116

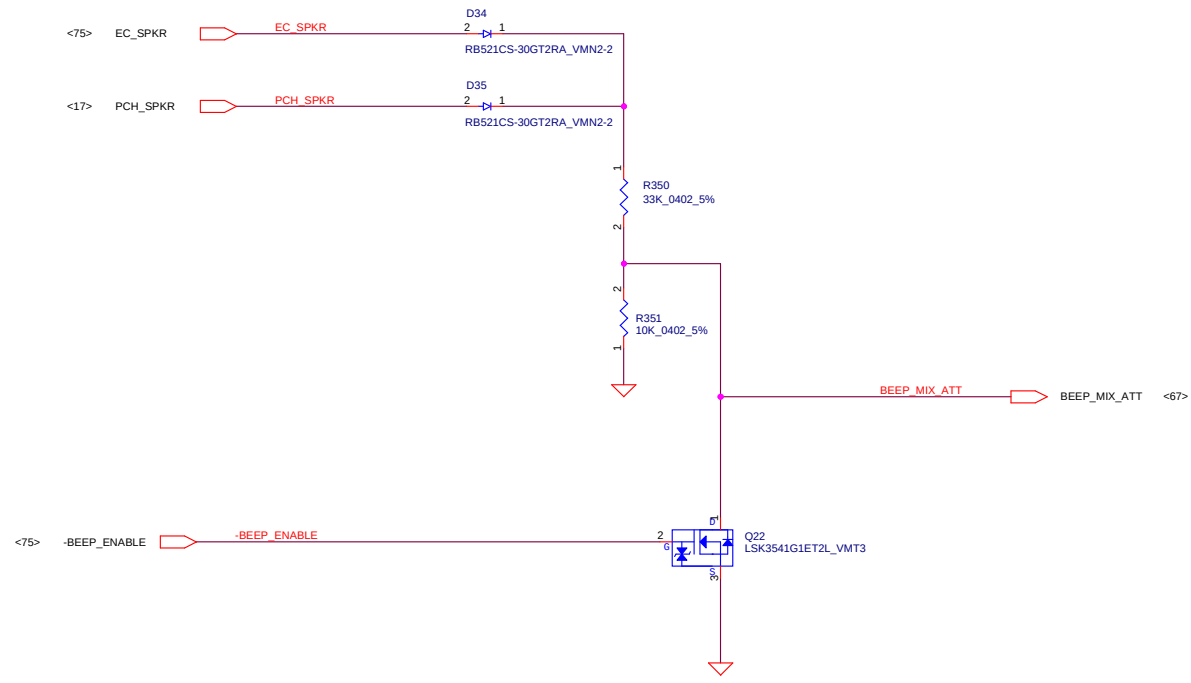


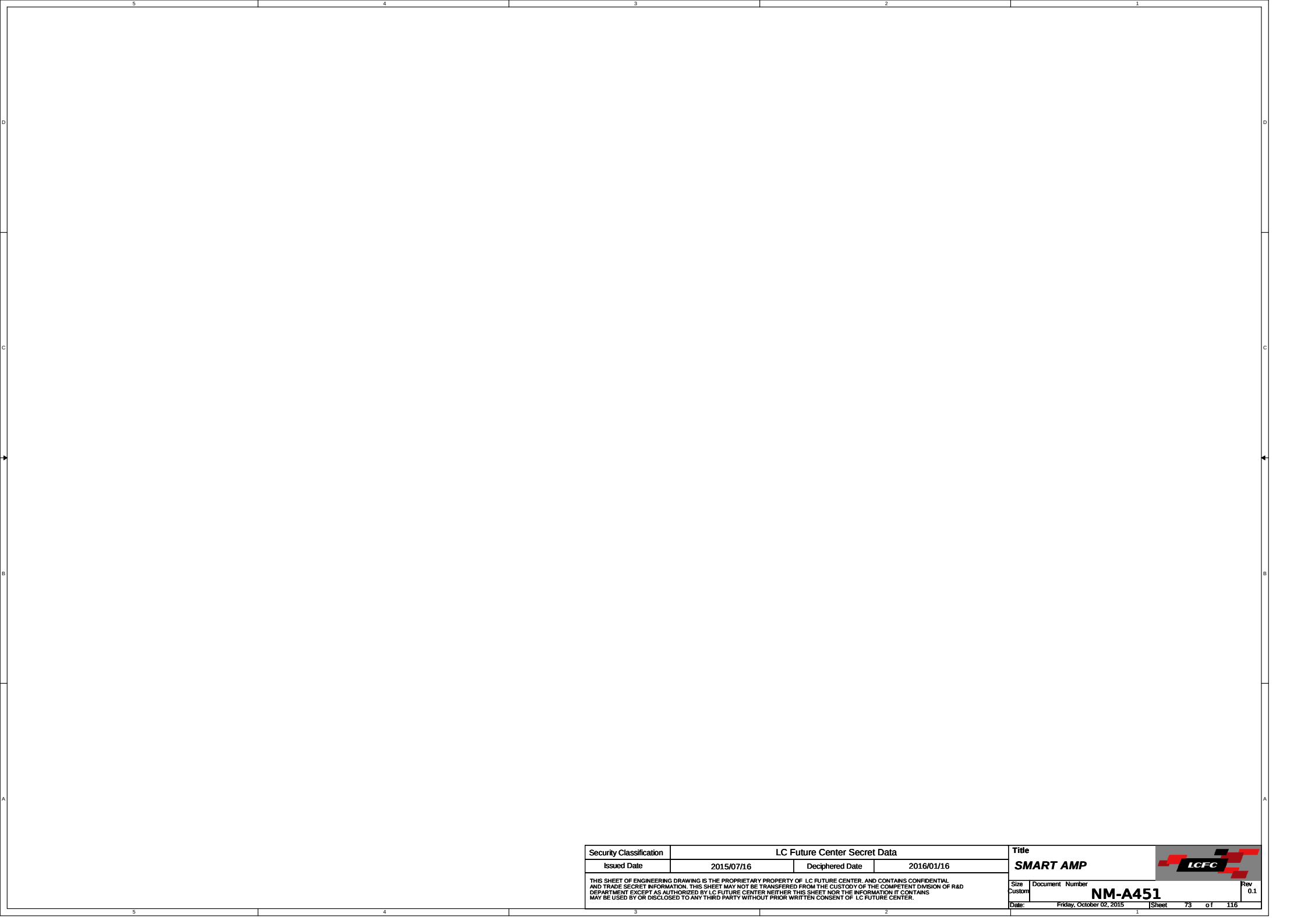



ALC3268 speaker output part

Speaker 4 ohm ==> 40 nls
Speaker 8 ohm ==> 20 nls

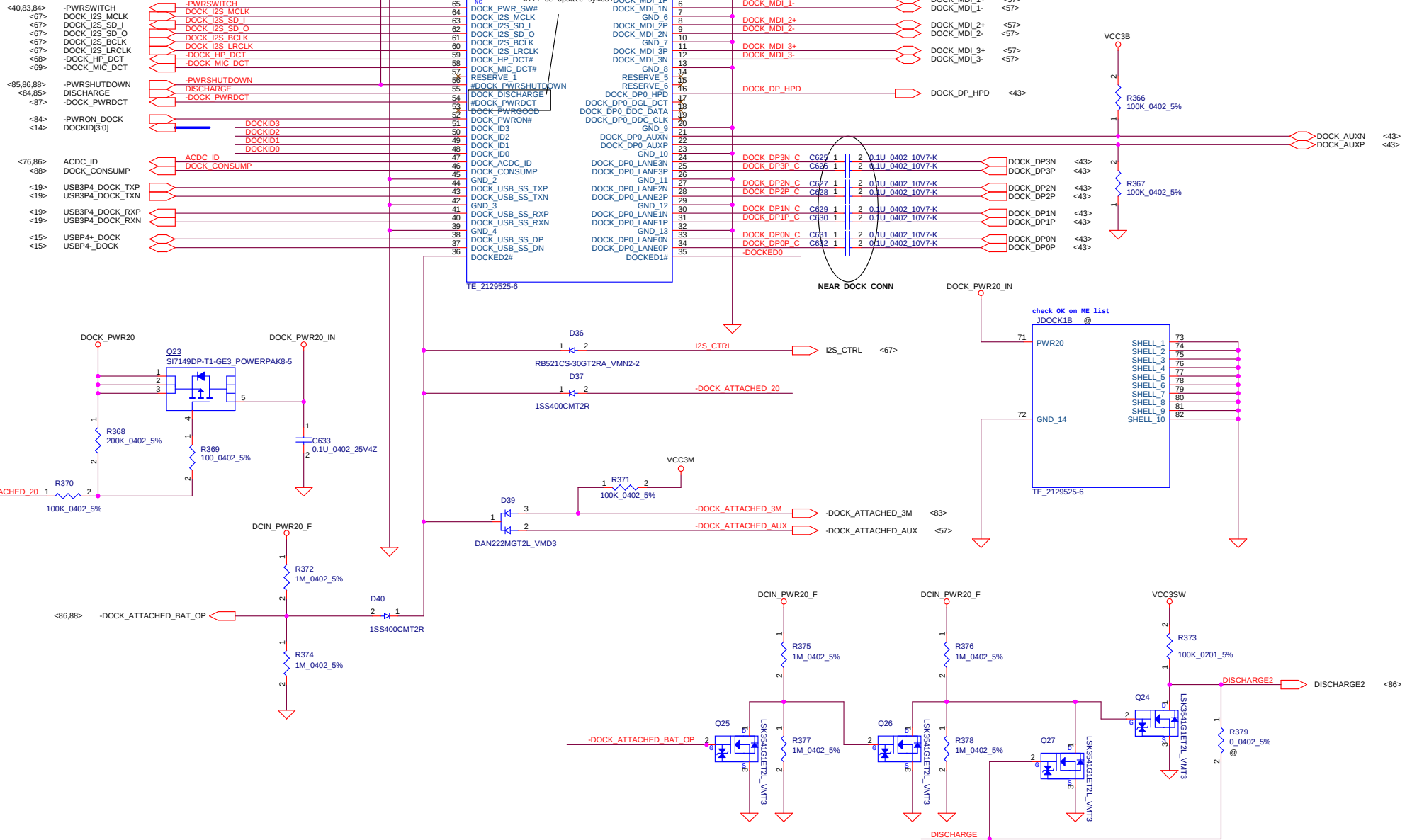


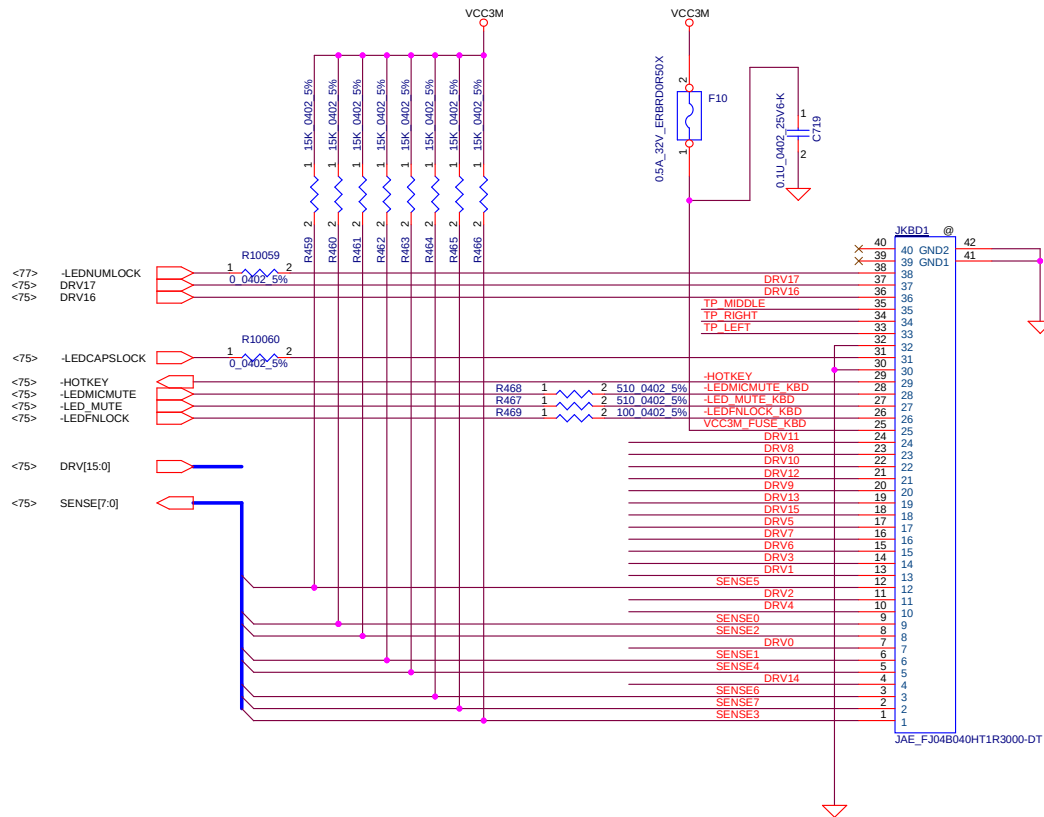




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Issued Date	2015/07/16	Deciphered Date	2016/01/16	SMART AMP			
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-PWRSHUTDOWN and DISCHARGE are not used in Thorpe. Payton needs these signals because system AC adapter can be attached even when docked.





<75> -KBD_BL_DTCT

<75> KBD_BL_PWM

<79> TP4CLK

<75,79> TP4_RESET

<79> TP4DATA

-KBD BL DTCT

KBD BL PWM

TP4CLK

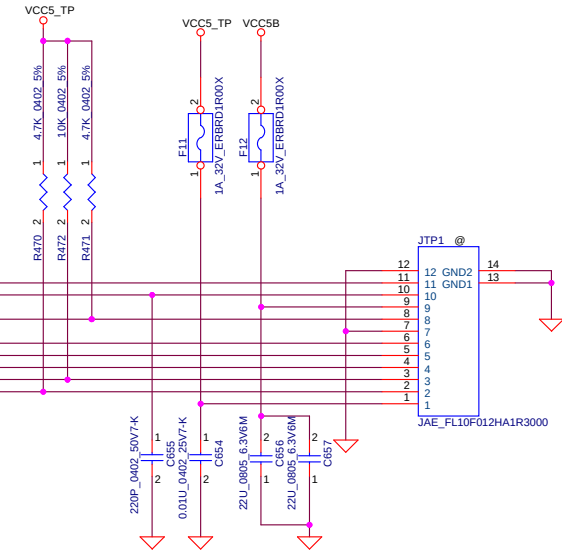
TP LEFT

TP RIGHT


TP MIDDLE

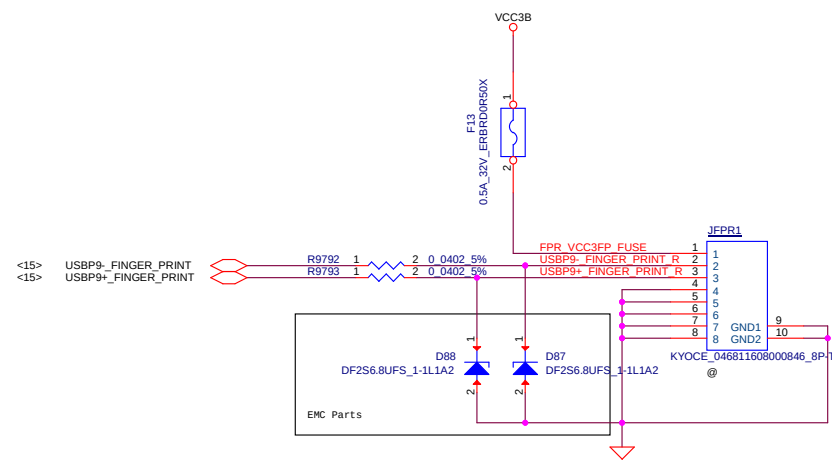
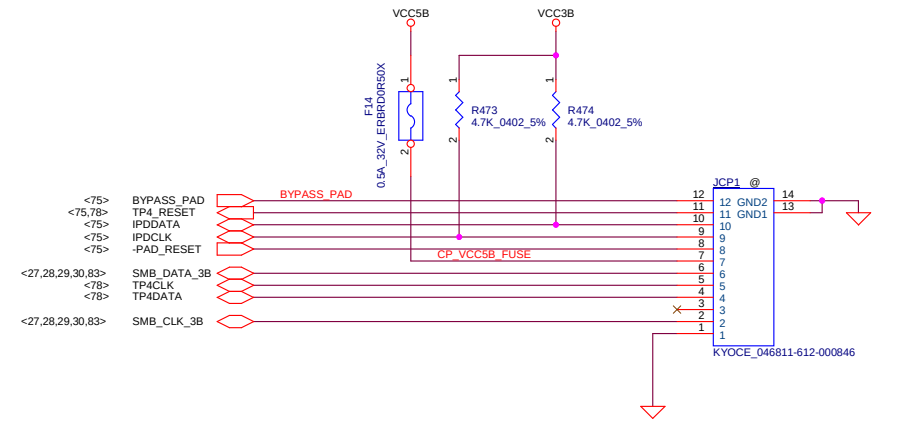
TP4_RESET

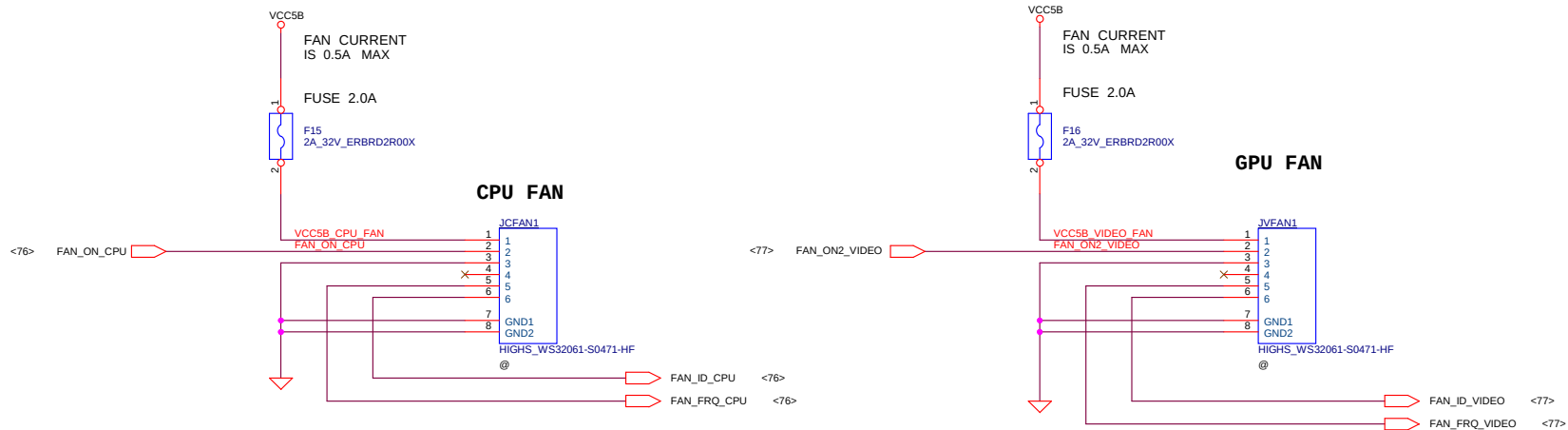
TP4DATA




Need confirm 5BCP conn
and change to symbol

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						Size		Document		Number		Rev	
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						Date:		Friday, October 02, 2015		Sheet 78 of 116			





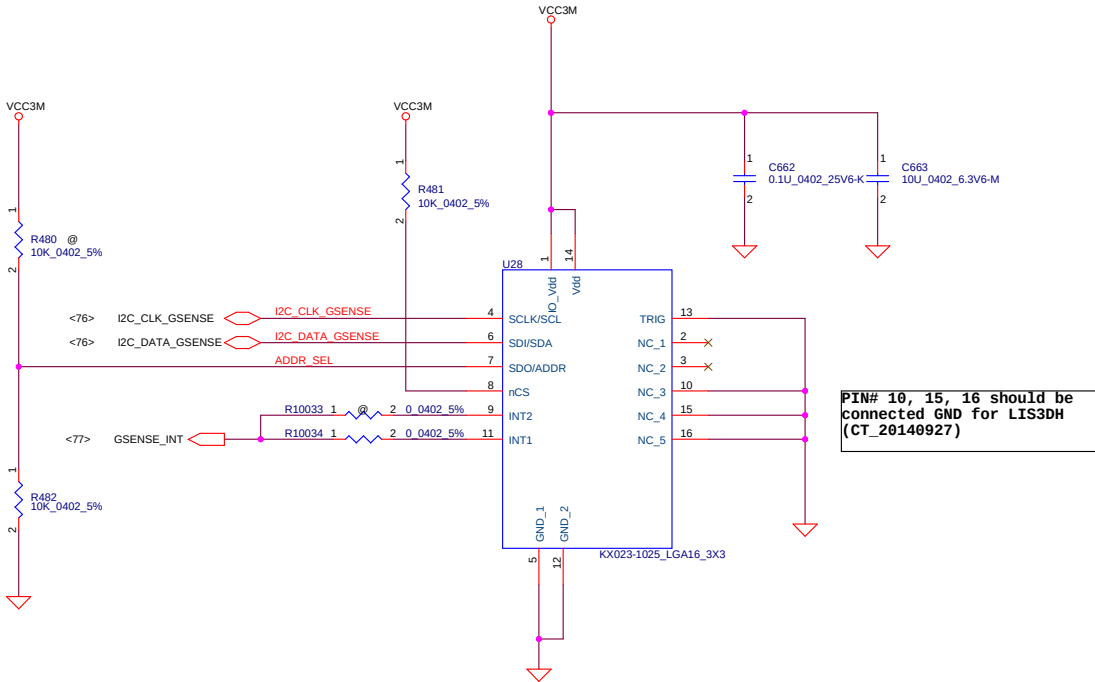
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Issued Date		Deciphered Date		FAN CONNECTOR			
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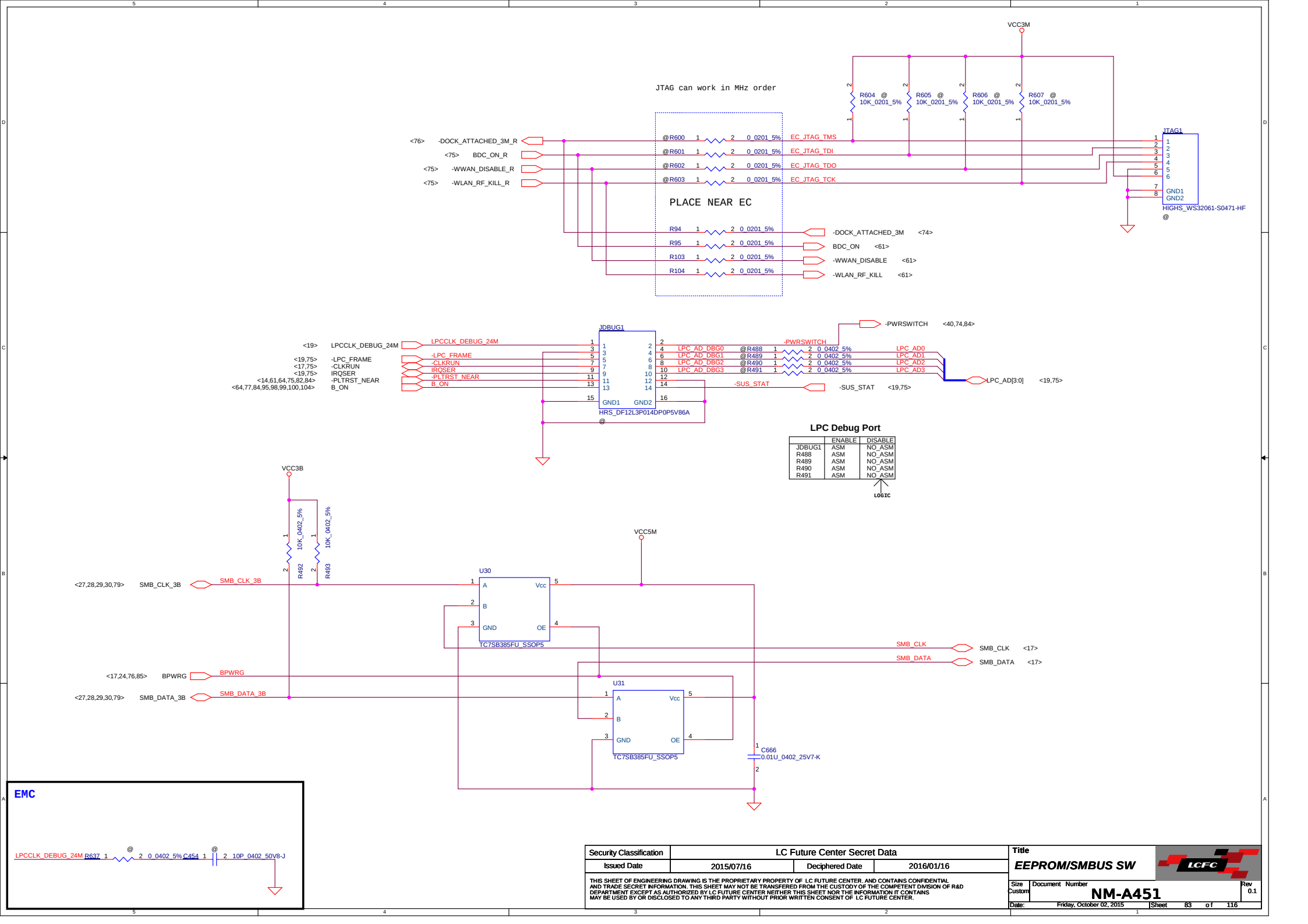
TABLE

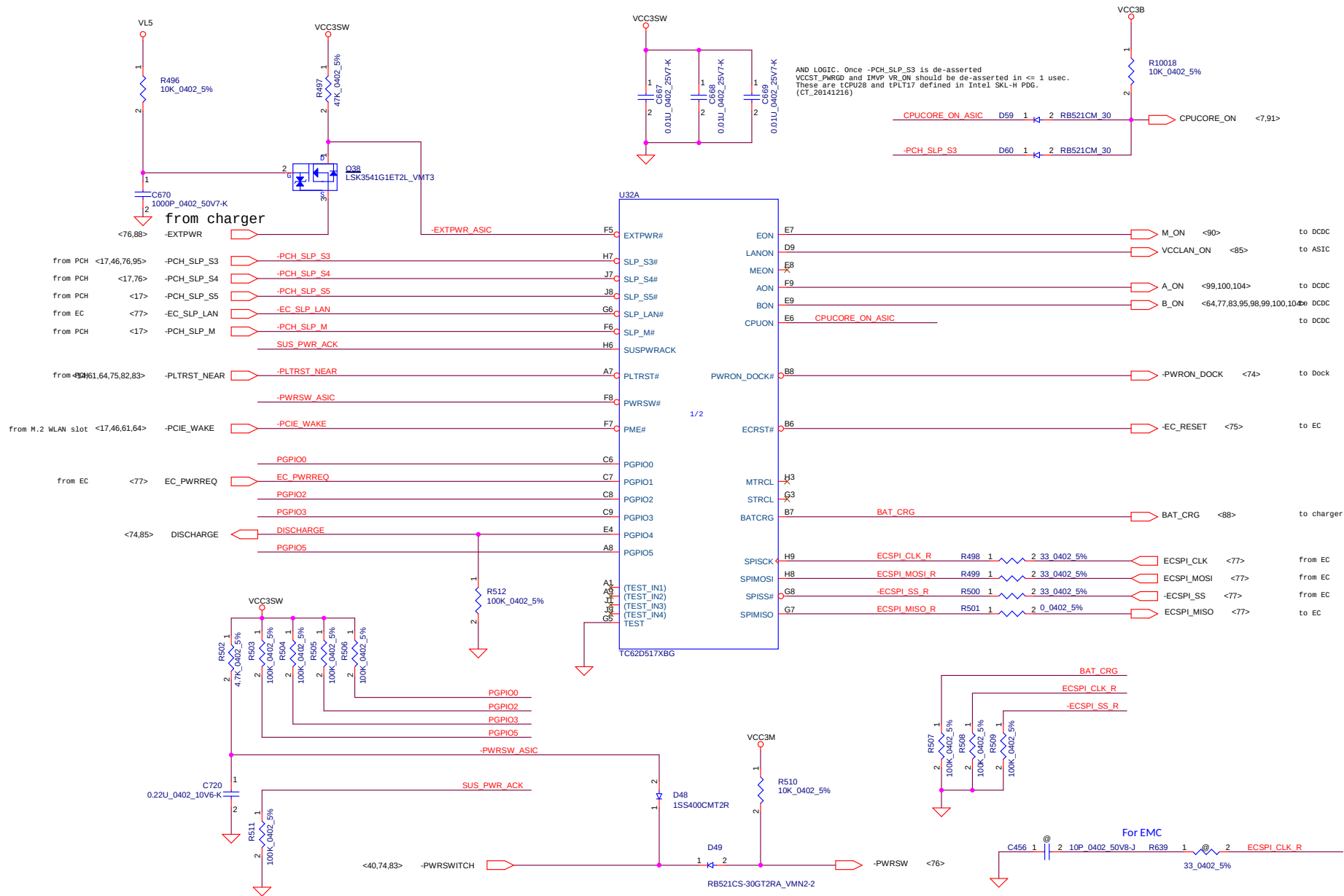
P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)


TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode







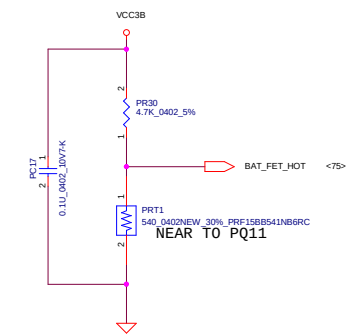
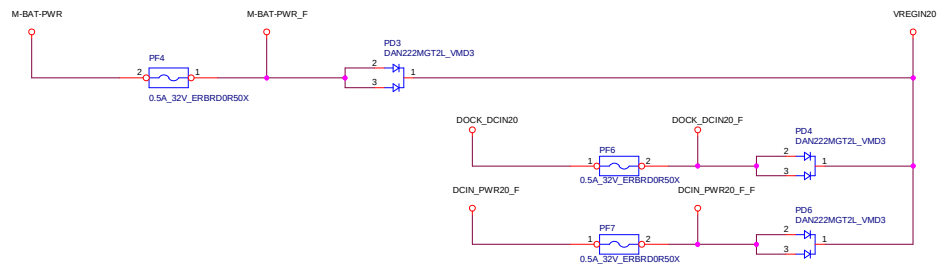
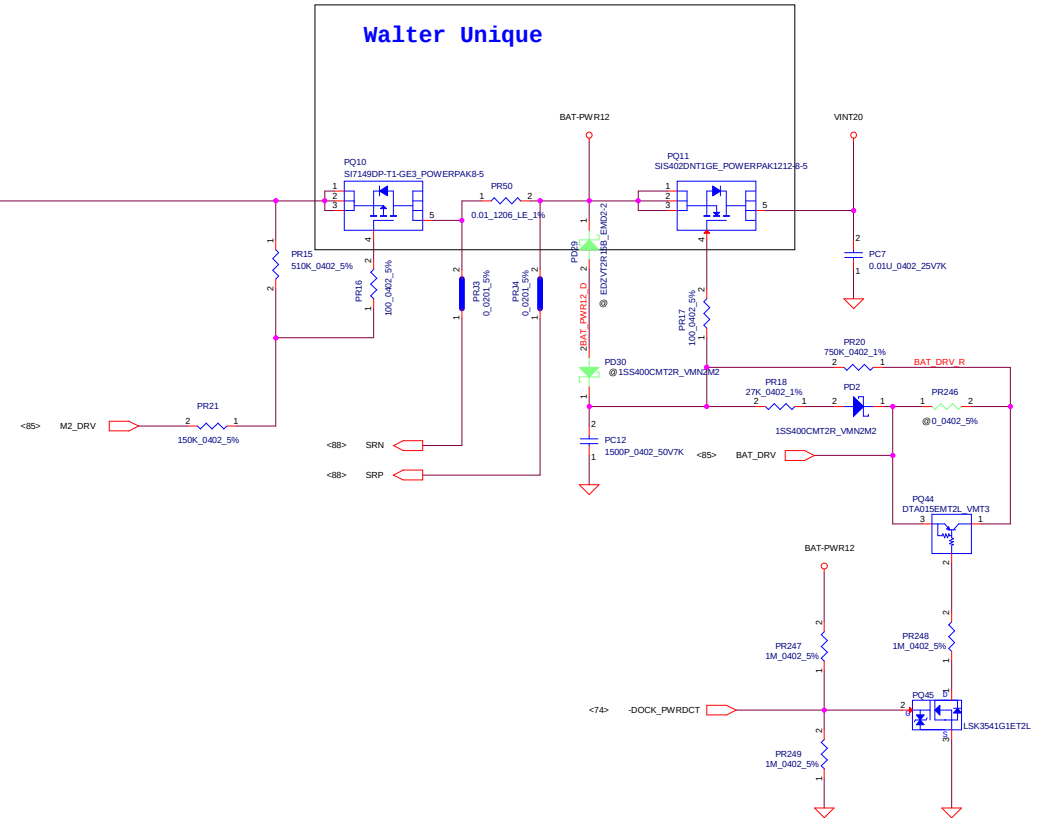
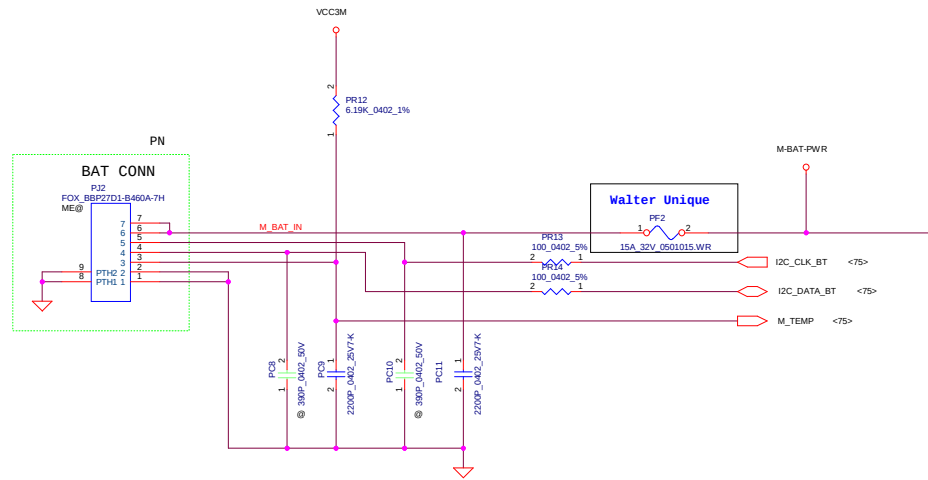
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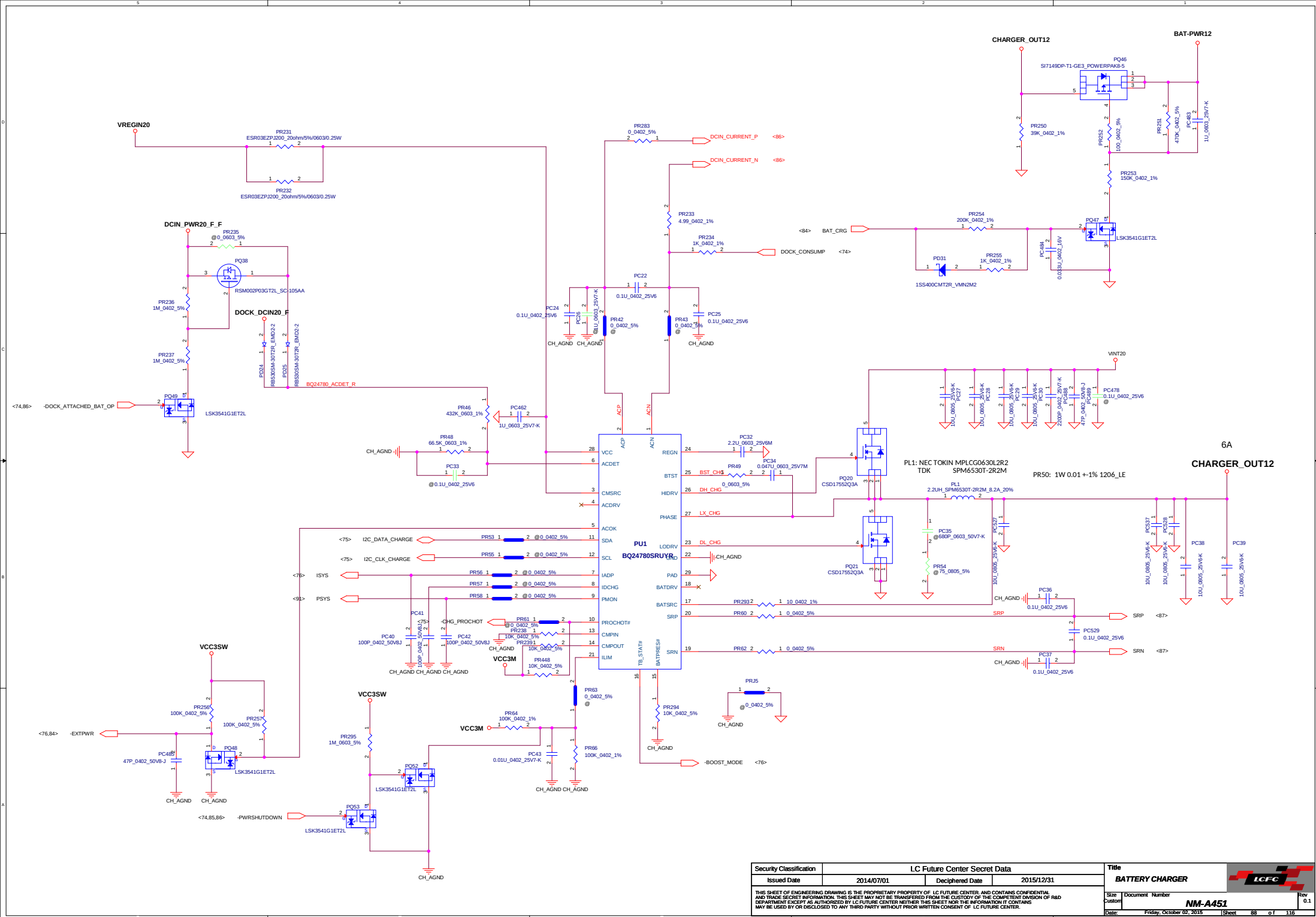
DCIN


SDV use PAYTON of SDV ,9-PIN Conn

TABLE		
PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM


LOGIC



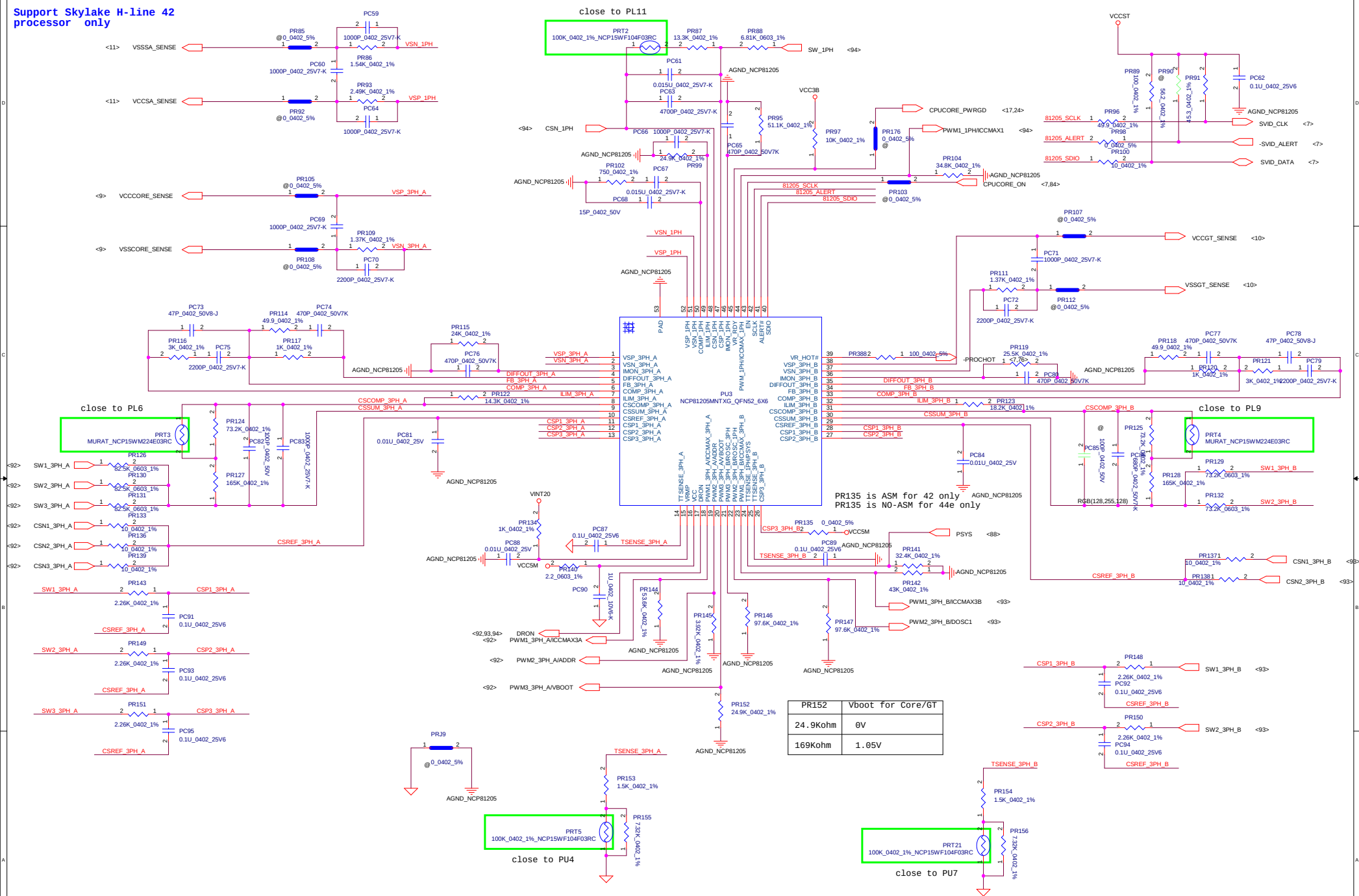



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Support Skylake H-line 42 processor only

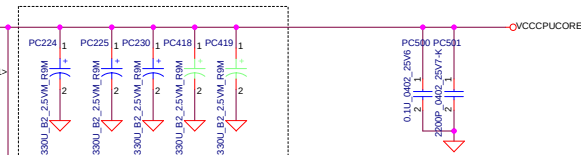
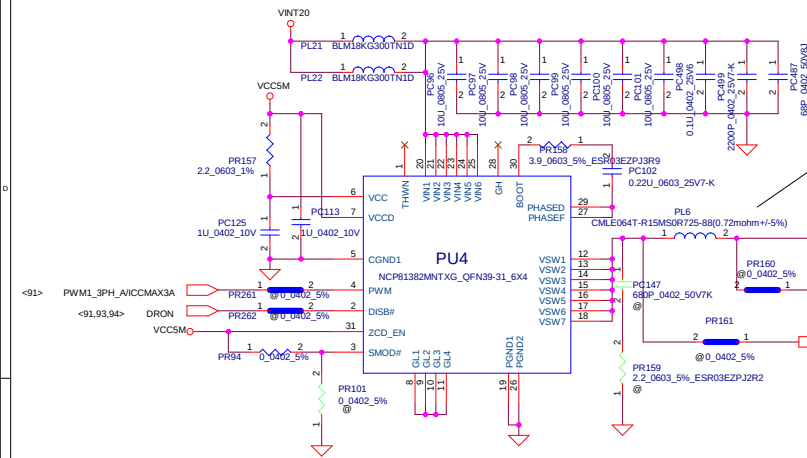


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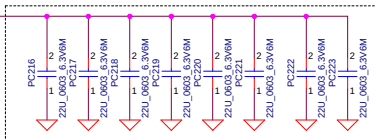
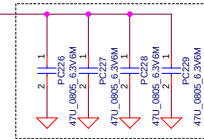
Support Skylake H-line 42 processor only

Cyntec:CMLE064T-R15MS0R725-88
Panasonic:ETQP4LR15AFM

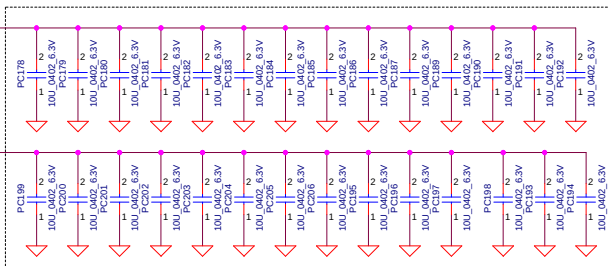
H42-45W
68A(TDC:56A)
H44e-45W
67A(TDC:56A)



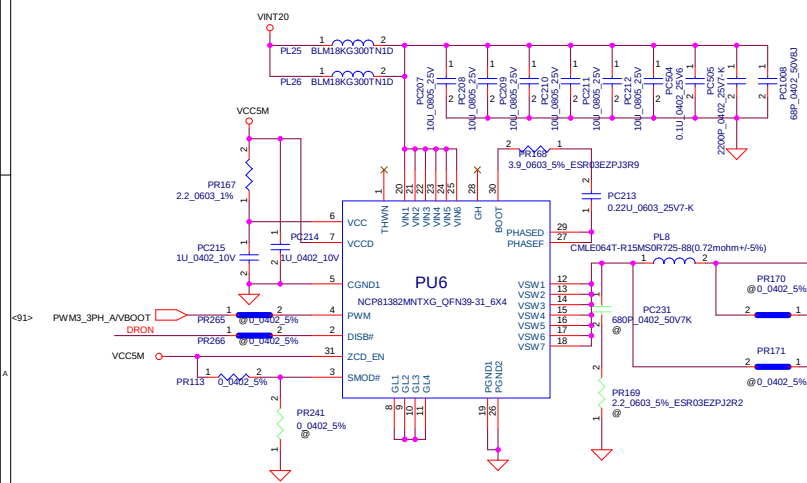
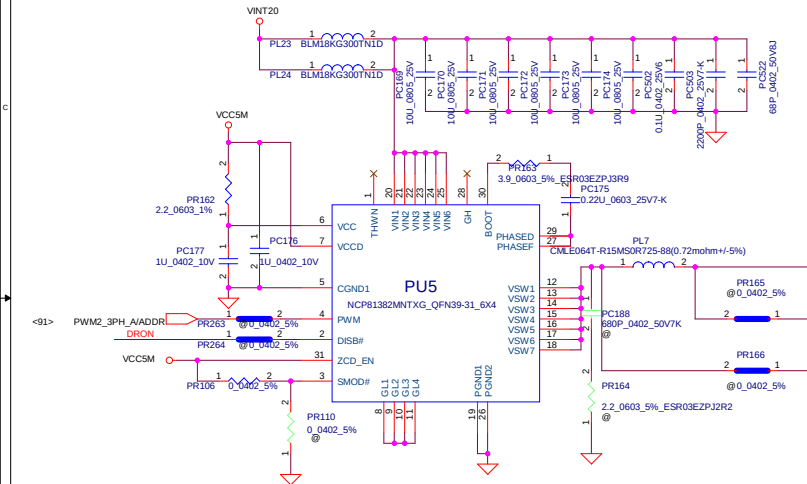
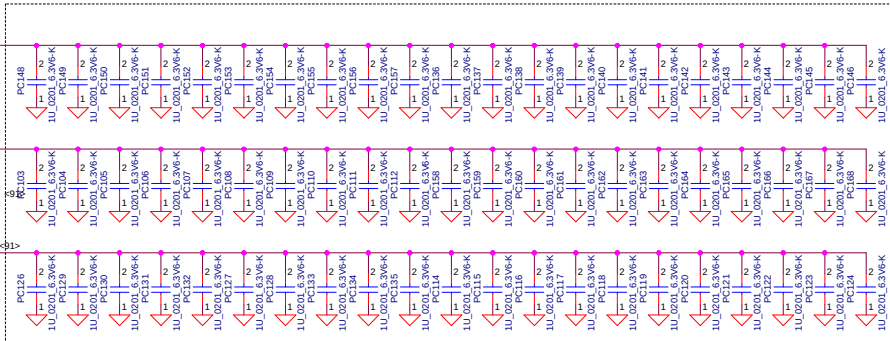
330uF 3pcs+2pcs(no mount)
47uF 4pcs




22uF 8pcs

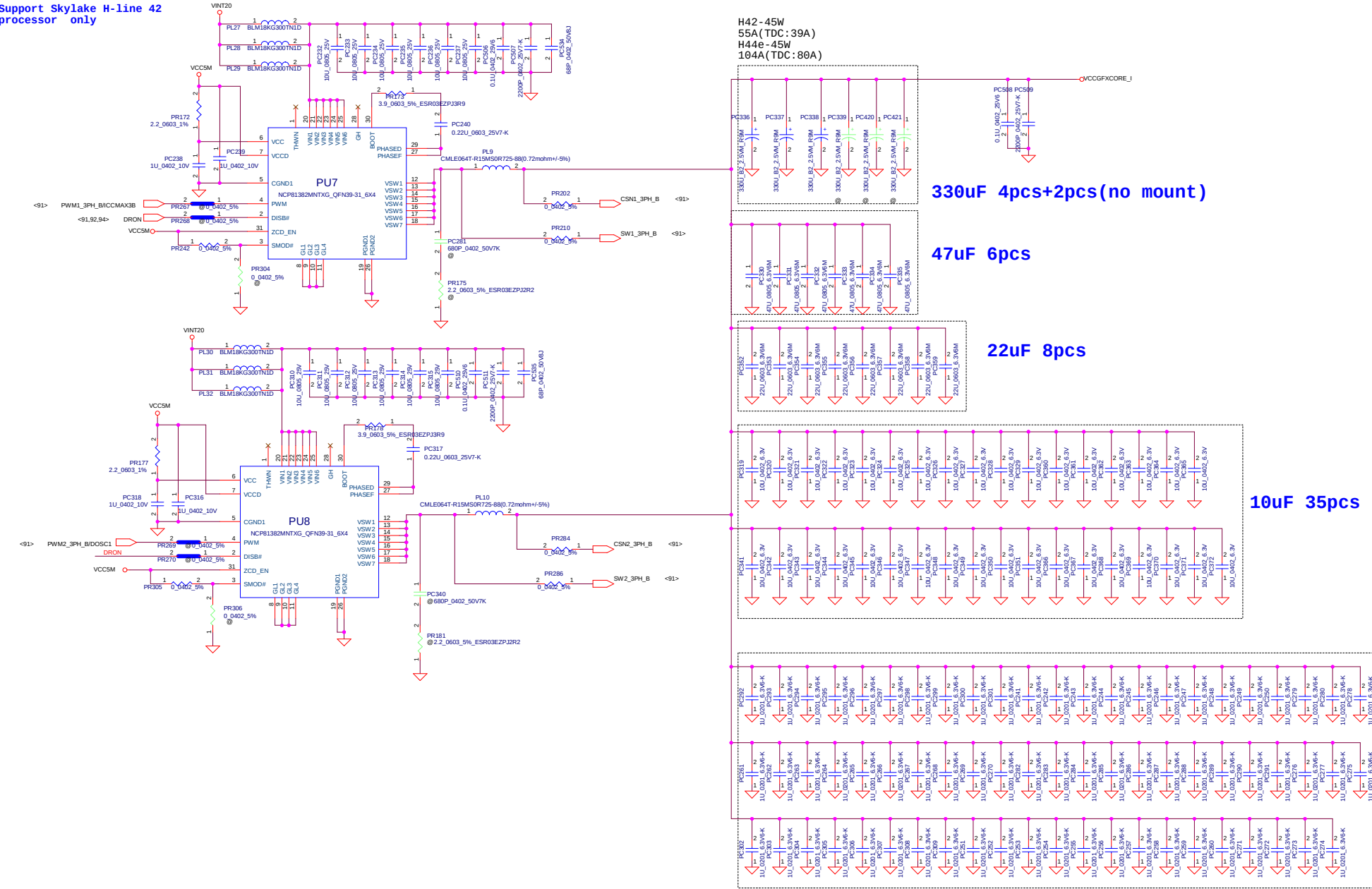


10uF 28pcs



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Support Skylake H-line 42
processor only



330uF 4pcs+2pcs(no mount)

47uF 6pcs


22uF 8pcs

10uF 35pcs

1uF 68pcs

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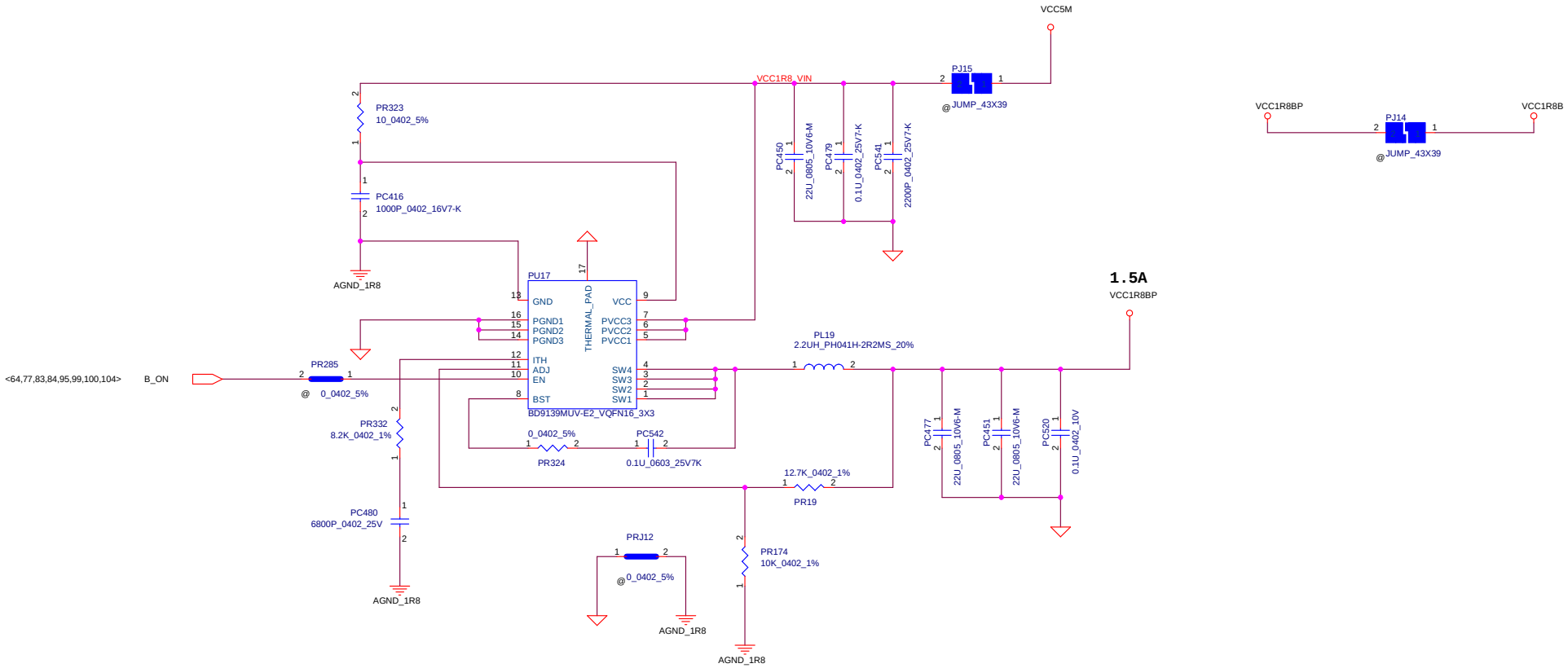


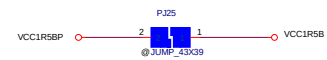
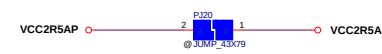
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0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975


LP#	C1	C0	VOUT (V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

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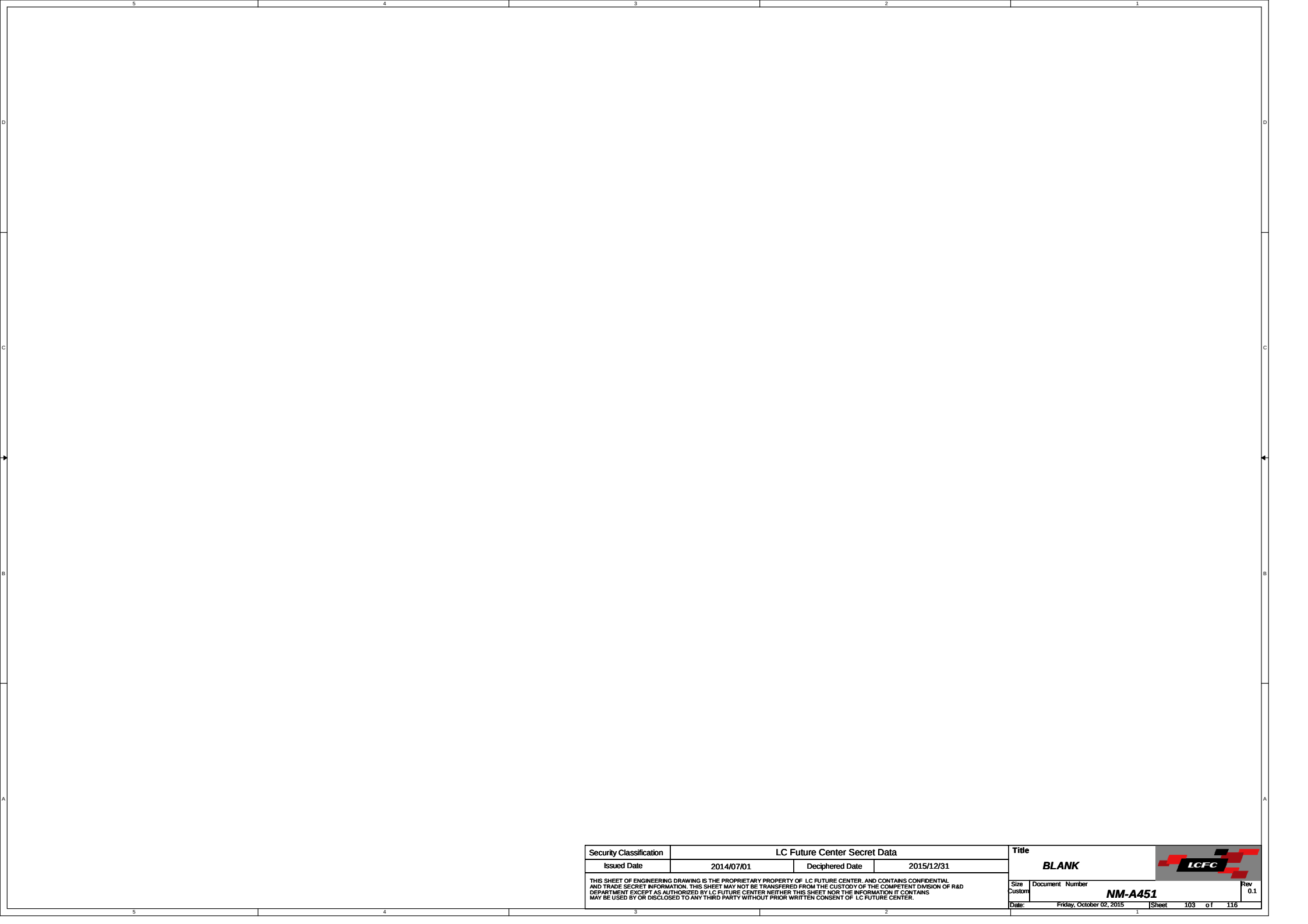
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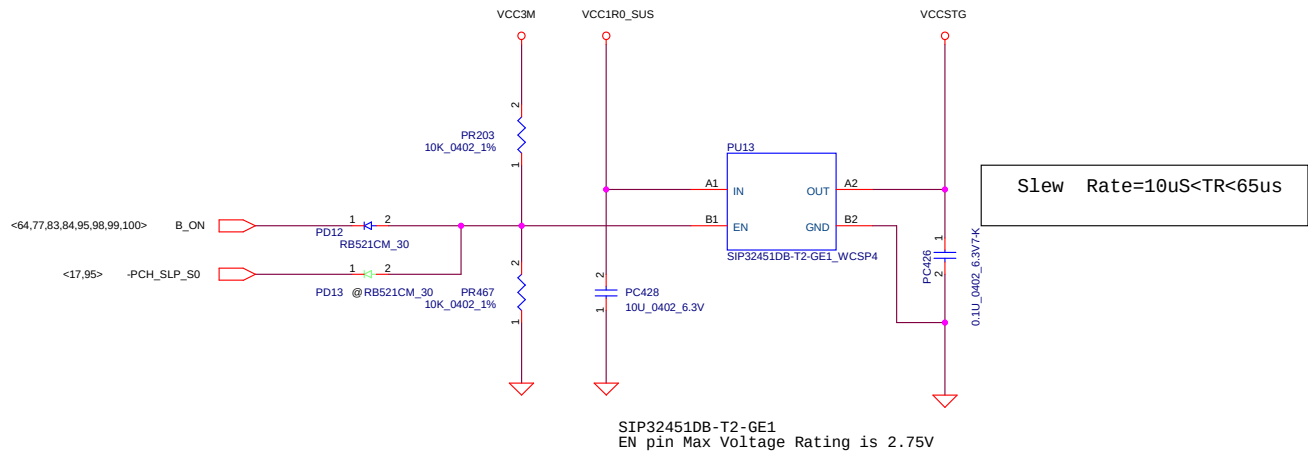
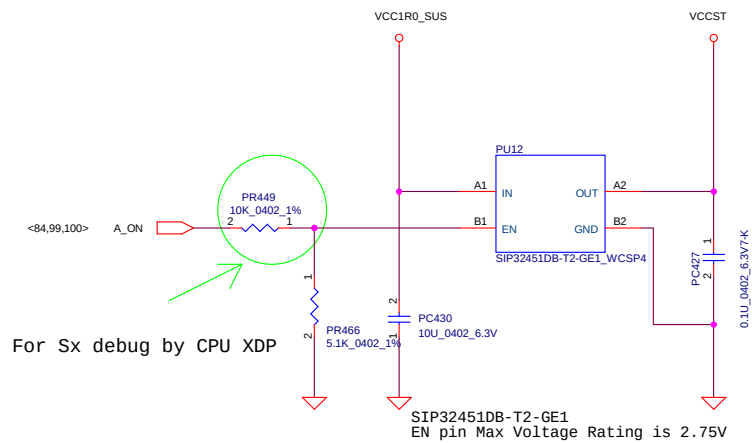
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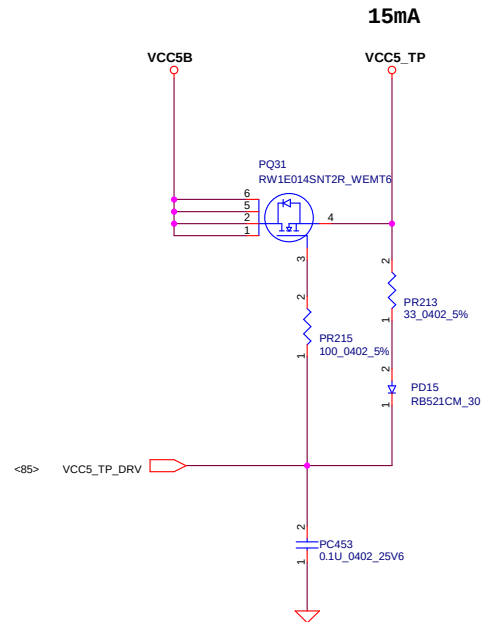
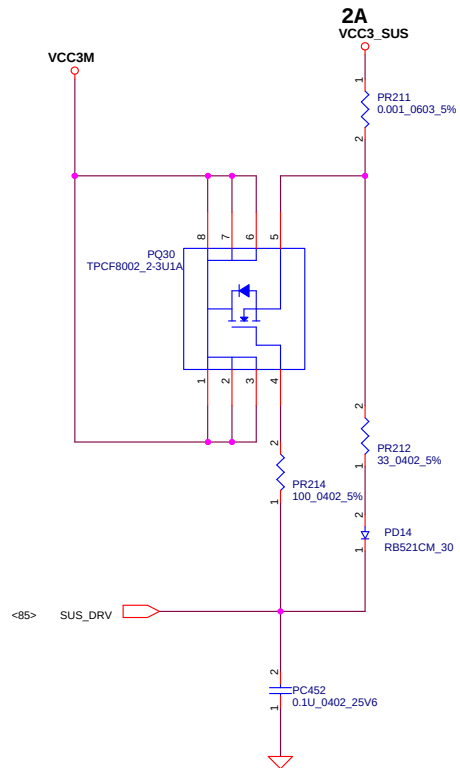
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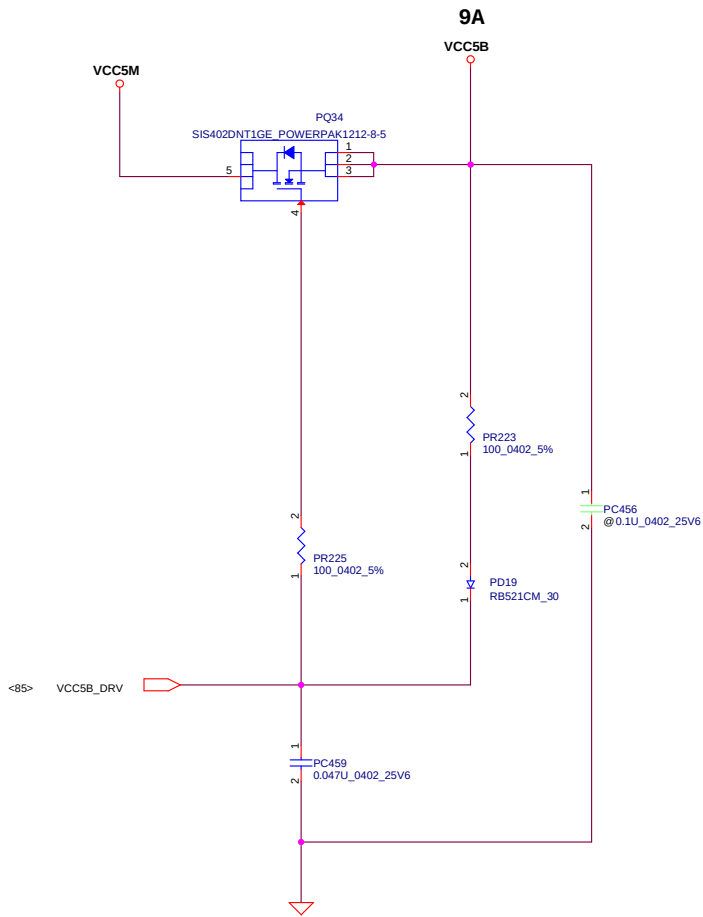
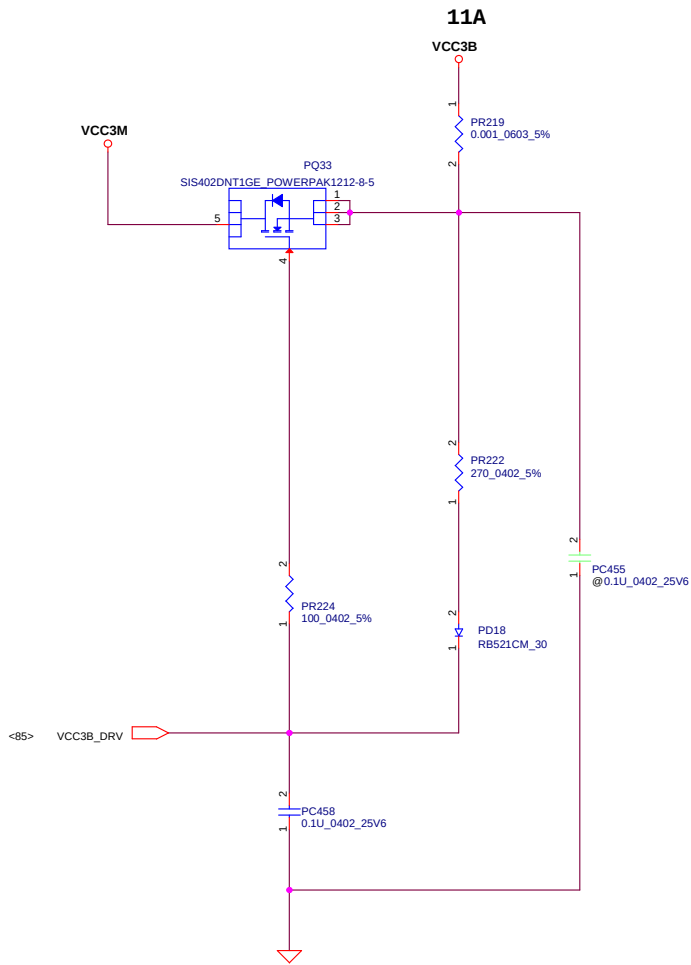


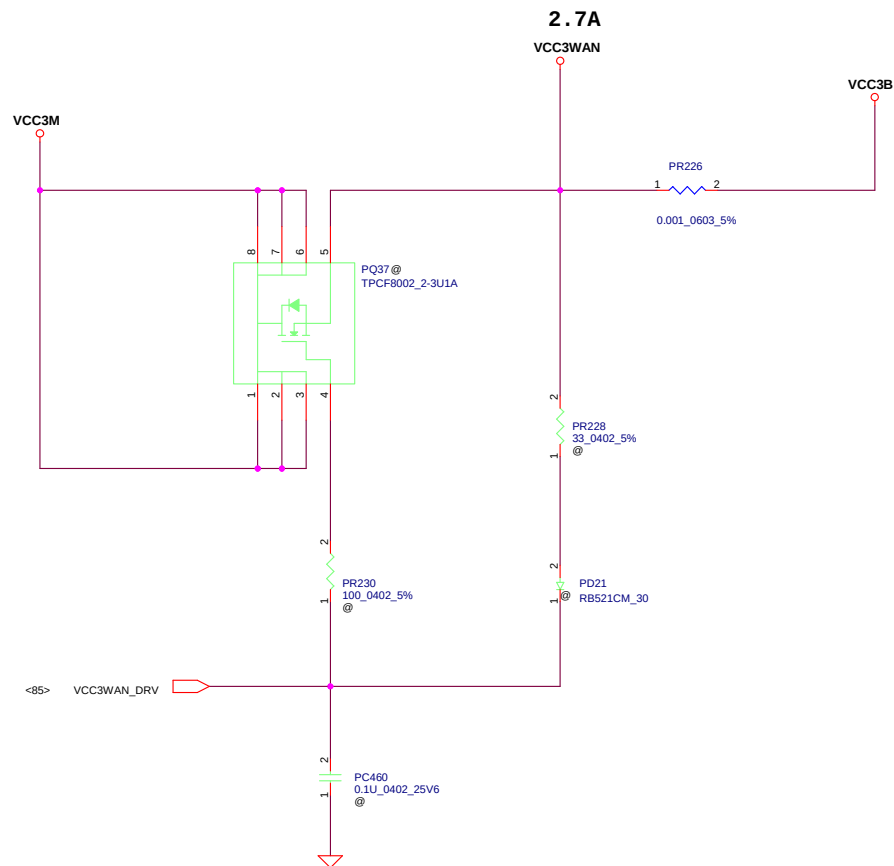
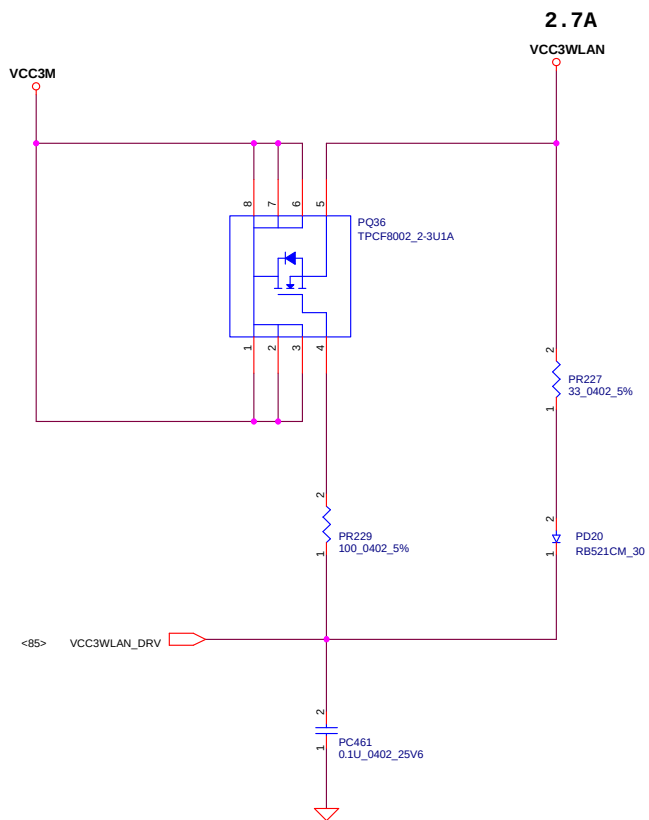
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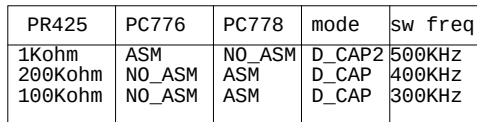






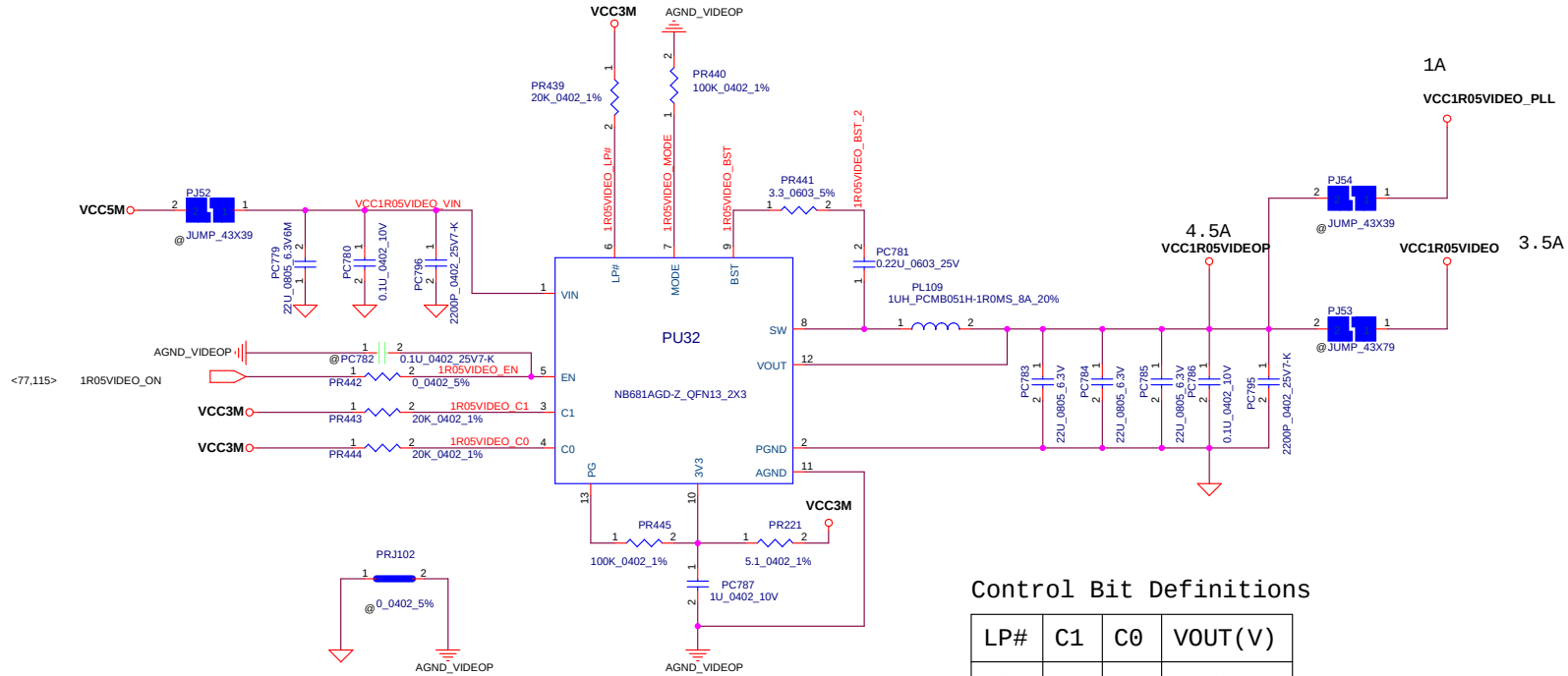
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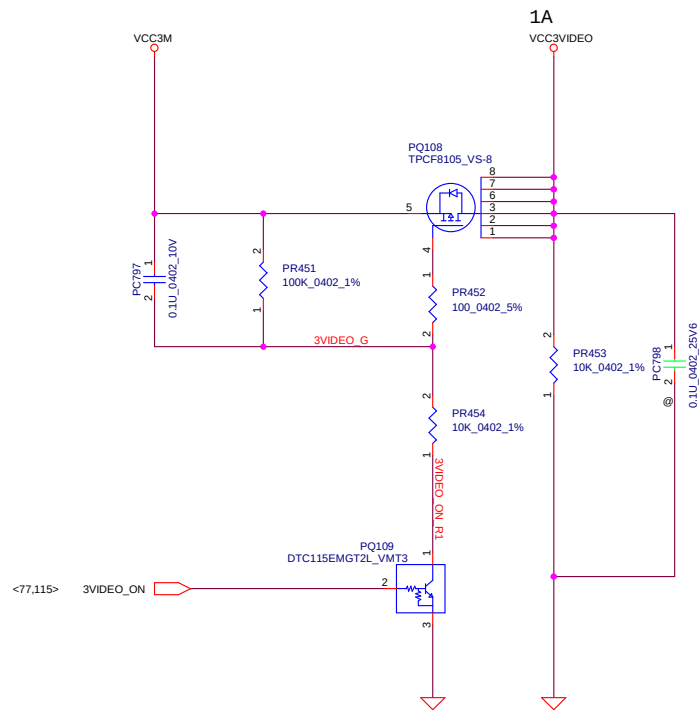



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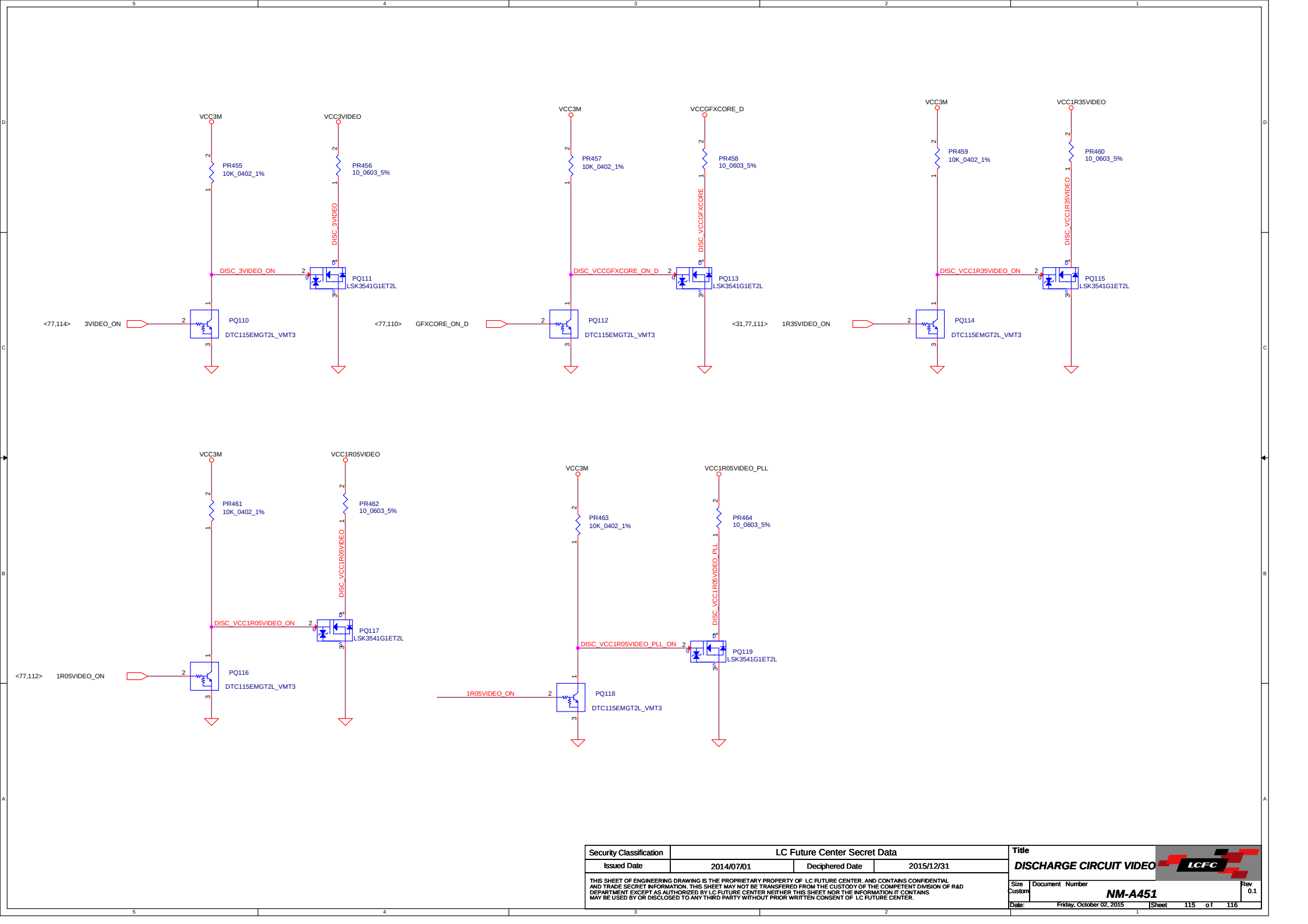
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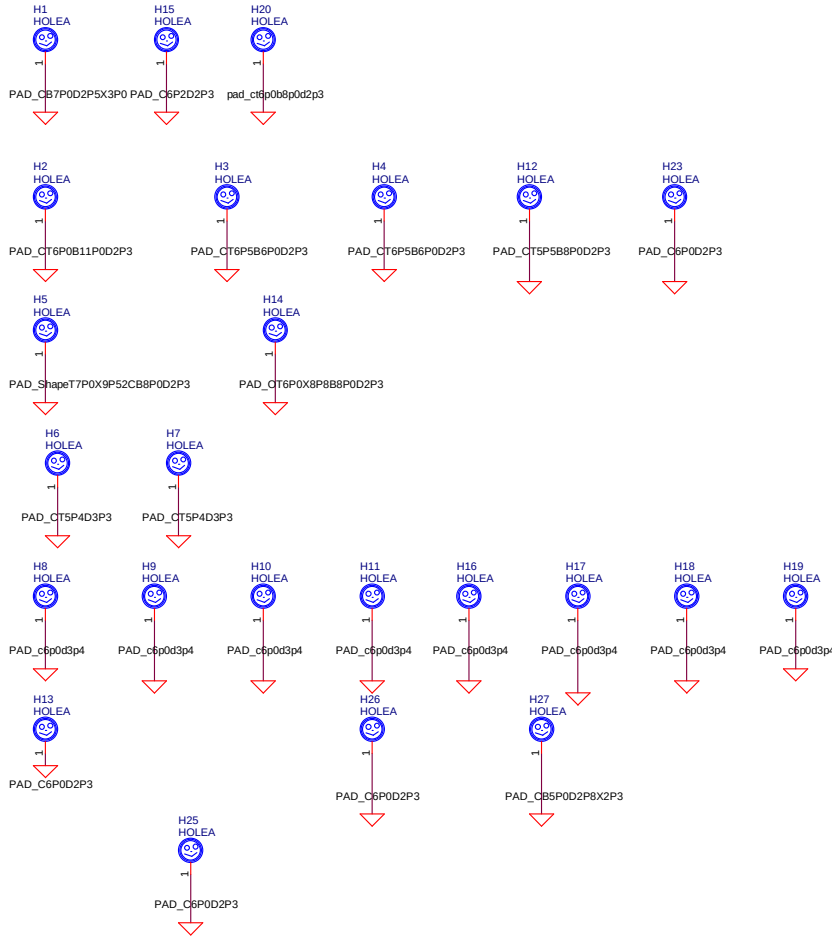
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